

Jaguar-1 SVT Planar Logic Schematics

JG1TL-3
VER 3.13
Dec/09/2020


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BASE LOGIC :

Jaguar-1 SIT Planar Logic Scchematics Ver.2.15

71.BLANK
72.DC INPUT
73.BATTERY INPUT
74.BATTERY CHARGER (BQ25710)
75.DC/DC VCC5M (NB690)
76.DC/DC VCC5_PD (NB693)
77.DC/DC VCC3M (TPS51393P)
78.LOAD SW VCC3_SUS
79.DC/DC VCC1R8_SUS (TLV62585)
80.DC/DC VCCPCHCORE (MP2941B)
81.DC/DC VCC1R1A/1R8A/0R6A (TPS51487X)
82.BLANK
83.DC/DC VCCCPUCORE (MP2940A)
84.DC/DC VCCCPUCORE (MP86941 X 2)
85.DC/DC VCCCPUCORE (MP86941 X 1)
86.LOAD SW VCCST & VCCSTG
87.BLANK
88.LOAD SW B
89.BLANK
90.BLANK
91.BLANK
92.BLANK
93.BLANK
94.LOAD SW TOUCH PANEL & SSD
95.PTH FOR SCREW HOLES
96.BLANK
97.BLANK

			
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EC HISTORY
JG1TL-3
(Base Logic : Jaguar-1 SIT Planar Logic Schematic Ver 2.15)

VER.3.00 2020/10/06 APPLIED JG1_SVT_EC001-EC002
VER.3.01 2020/10/08 APPLIED JG1_SVT_EC003-EC005
VER.3.02 2020/10/12 APPLIED JG1_SVT_EC006-EC010
VER.3.03 2020/10/13 APPLIED JG1_SVT_EC011
VER.3.04 2020/10/14 APPLIED JG1_SVT_EC012
VER.3.06 2020/10/21 APPLIED JG1_SVT_EC013
VER.3.07 2020/11/03 APPLIED JG1_SVT_EC0014-EC015
VER.3.08 2020/11/05 APPLIED JG1_SVT_EC0016
VER.3.09 2020/11/08 APPLIED JG1_SVT_EC0017
VER.3.10 2020/11/13 APPLIED JG1_SVT_EC0018
VER.3.11 2020/11/17 APPLIED JG1_SVT_EC0019
VER.3.12 2020/11/26 APPLIED JG1_SVT_EC0020
VER.3.13 2020/12/09 APPLIED JG1_SVT_EC0021

LCFC 3Pin Symbol rule
Orcad Symbol & PCB Footprint pin assignment

Use common rule, Top side is Pin1, not follow original
datasheet definition to avoid confusion with different
vender definition. Below is an example.

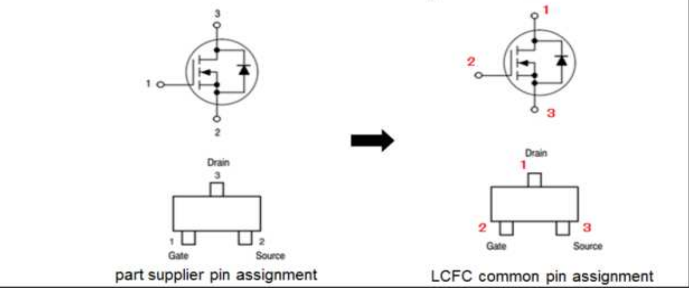


TABLE: Chip Capacitor Thermal Characteristics

		Code
-55 to 150degC	+/-30ppm/degC	NPO
-55 to 125degC	+/-30ppm/degC	C0G
-55 to 125degC	+/-15%	X7R
-55 to 105degC	+/-22%	X6S
-55 to 85degC	+/-15%	X5R

TABLE: Chip Capacitor Tolerance

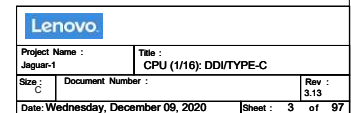
Tolerance	Code
+/-0.1pF	B
+/-0.25pF	C
+/-0.5pF	D
+/-5%	J
+/-10%	K
+/-20%	M
+80/-20%	Z

TABLE: Chip Part Dimension

Size [mm]	mm Size Code	Inch Size Code
0.40 x 0.20	0402	01005
0.60 x 0.30	0603	0201
1.00 x 0.50	1005	0402
1.60 x 0.80	1608	0603
2.00 x 1.25	2125	0805
2.00 x 1.60	2016	0806
2.50 x 2.00	2520	1008
3.20 x 1.60	3216	1206
3.20 x 2.50	3225	1210
4.50 x 1.60	4516	1806
4.50 x 2.50	4525	1810
4.50 x 3.20	4532	1812
5.00 x 2.50	5025	2010
6.40 x 3.20	6432	2512

↑
LOGIC

GPP_E19/DDP1_CTRLDATA/TBT_LXS0_RXD (DDP1 I2C / TBT_LXS0 Pin VCC Configuration)	
GPP_E21/DDP2_CTRLDATA/TBT_LXS1_RXD (DDP2 I2C / TBT_LXS1 Pin VCC Configuration)	
GPP_D10/DDP3_CTRLDATA/TBT_LXS2_RXD (DDP3 I2C / TBT_LXS2 Pin VCC Configuration)	
GPP_D12/DDP4_CTRLDATA/TBT_LXS3_RXD (DDP4 I2C / TBT_LXS3 Pin VCC Configuration)	
HIGH	3.3V for HDMI Display I2C (External Pull-Up Resistor Required)
LOW	1.8V for Thunderbolt LSX (Default)



SPI0_MOSI (Boot Halt)	
HIGH	Disabled
LOW	Enabled

← LOGIC

SPI0_I02 (Consent Strap)	
HIGH	Disabled
LOW	Enabled

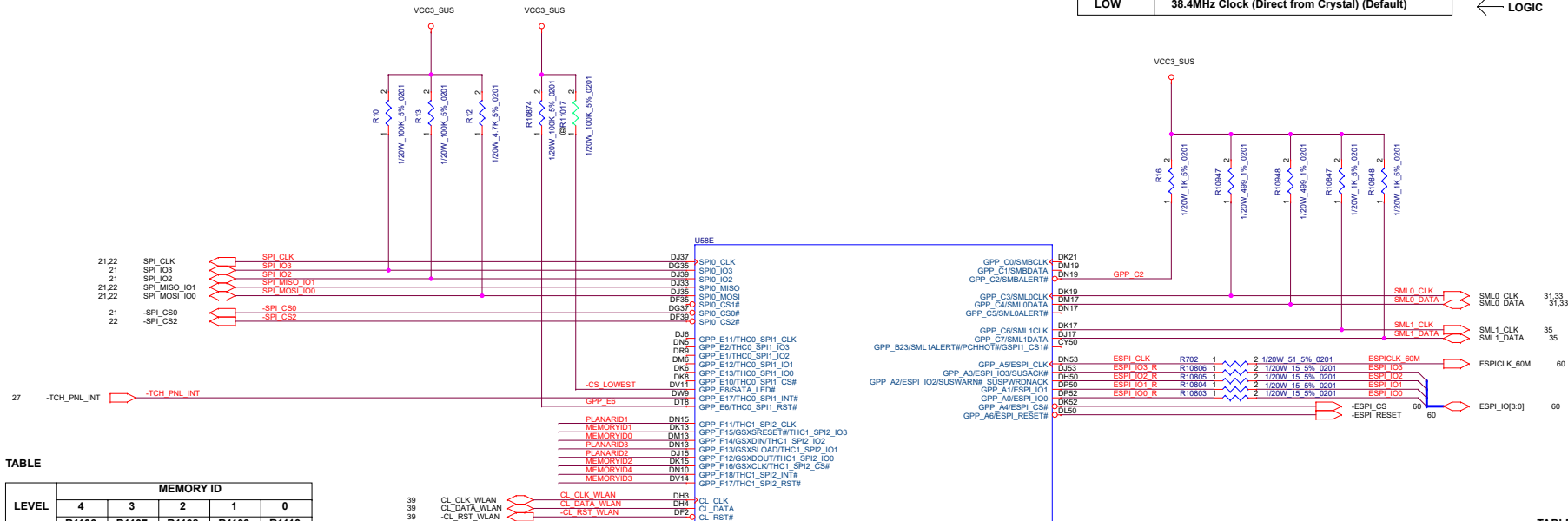
← LOGIC

SPI0_IO3 (A0 Personality Strap)	
HIGH	Disabled
LOW	Enabled

← LOGIC

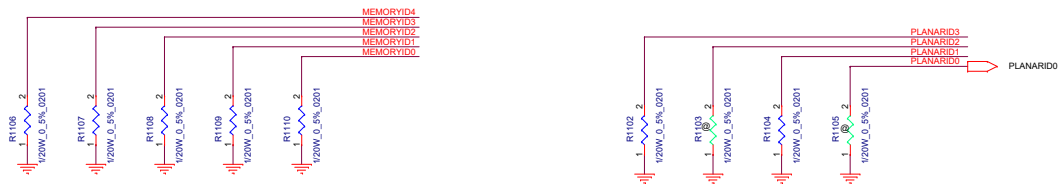
GPP_E6 (JTAG ODT Disable)	
HIGH	JTAG ODT Enabled
LOW	JTAG ODT Disabled

← LOGIC



LEVEL	MEMORY ID				
	4	3	2	1	0
	R1106	R1107	R1108	R1109	R1110
1	NA	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM	ASM

MEMORYID[4:0]	U275,U276,U277,U278				Total Memory
	Supplier	Supplier's P/N	Capacity		
00h (00000b)	SK hynix	H9HCNNNBKMLXR-NEE	16Gb	DDP	8GB
01h (00001b)		H9HCNNNCPMLXR-NEE	32Gb	QDP	16GB
02h (000010b)		H9HCNNNFAMMLXR-NEE	64Gb	ODP	32GB
03h (00011b)	Samsung	K4U6E3S4AA-MGCR	16Gb	SDP	8GB
04h (00100b)		K4UBE3D4AA-MGCR	32Gb	DDP	16GB
05h (00101b)		K4UCCE3Q4AA-MGCR	64Gb	QDP	32GB
06h (00110b)	Micron	MT53E51M232D2NP-046 WT-E	16Gb	DDP	8GB
07h (00111b)		MT53E1G32D2NP-046 WT-A	32Gb	DDP	16GB
08h (01000b)		MT53E2G32D4NQ-046 WT-A	64Gb	QDP	32GB



GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

← LOGIC

GPP_C5/SML0ALERT# (Boot Strap Bit 0)	
GPP_H0 (Boot Strap Bit 1)	
GPP_H1 (Boot Strap Bit 2)	
GPP_H2 (Boot Strap Bit 3)	
0000b	Master Attached Flash Configuration (Default)

GPP_B23/SML1ALERT#/PCHHOT# (CPUNSSC Clock Frequency)	
HIGH	19.2MHz Clock (Derived from 38.4MHz Crystal)
LOW	38.4MHz Clock (Direct from Crystal) (Default)

← LOGIC

LEVEL	PLANAR ID			
	3	2	1	0
	R1102	R1103	R1104	R1105
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

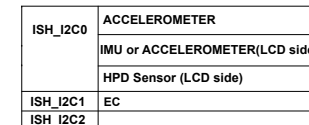
LEVEL	PLANARID[3:0]
EVT	0000B
ME-FVT	0001B
FVT	0010B
ME-SIT	0011B
SIT	0100B
SVT	0101B

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" mode
LOW	Disable "Top Swap" mode (Default)

ISH I2C1: 3.3V

GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)

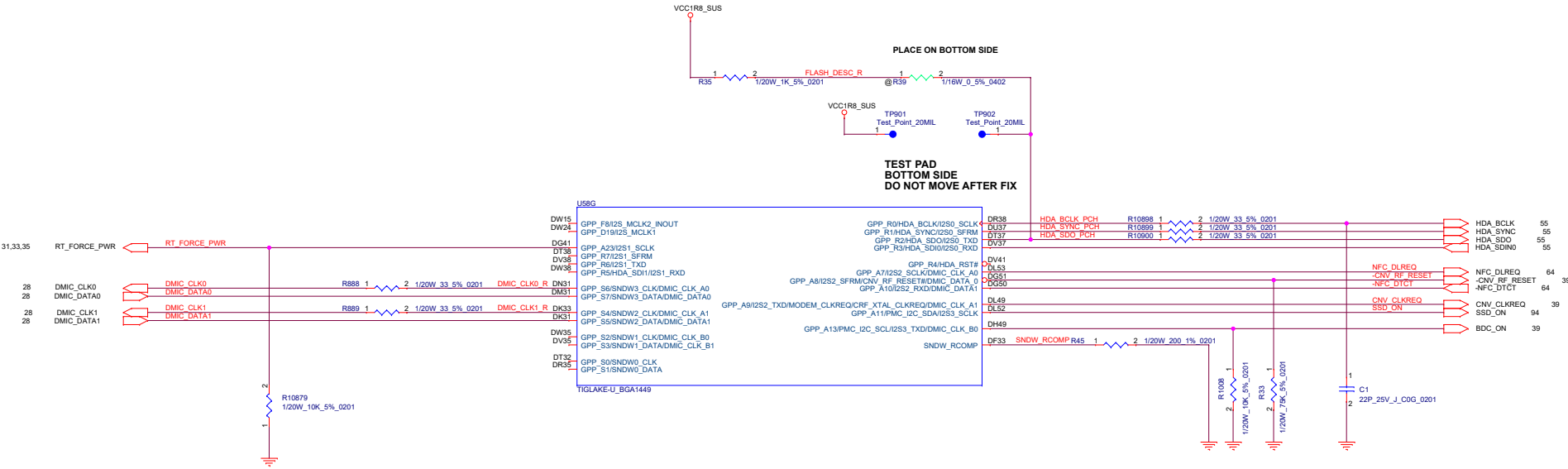
VCC1R8_SUS



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TABLE : Functional Strap

GPP_R2/HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)



Flexible I/O Configuration								
HSIO Port	High Speed Signals	PCI		HSIO Configuration	Descriptor for PCIe	Net Name	PCI	
		Device	Function				Device	Function
PCH L0	USB 3.1 #1 / PCIe Gen3 #1	1Ch	0h	USB 3.1 #1	1x2, 2x1 Lane Reversal Enabled	USB3_P1	14h	0h
PCH L1	USB 3.1 #2 / PCIe Gen3 #2		1h	USB 3.1 #2		USB3_P2		
PCH L2	USB 3.1 #3 / PCIe Gen3 #3		2h	PCIe Gen3 #3		PCIE3_P1_L1		
PCH L3	USB 3.1 #4 / PCIe Gen3 #4		3h	PCIe Gen3 #4		PCIE3_P1_L0		
PCH L4	PCIe Gen3 #5	1Ch	4h	PCIe Gen3 #5	4x1 Lane Reversal Disabled	PCIE3_P5	1Ch	4h
PCH L5	PCIe Gen3 #6		5h	PCIe Gen3 #6		N/A		
PCH L6	PCIe Gen3 #7 (GbE)		6h	PCIe Gen3 #7		N/A		
PCH L7	PCIe Gen3 #8 (GbE)		7h	PCIe Gen3 #8		N/A		
PCH L8	PCIe Gen3 #9 (GbE)	1Dh	0h	PCIe Gen3 #9 (x4)	1x4 Lane Reversal Disabled	N/A		
PCH L9	PCIe Gen3 #10		1h	PCIe Gen3 #10 (x4)		N/A		
PCH L10	PCIe Gen3 #11 / SATA #0		2h	PCIe Gen3 #11 (x4)		N/A		
PCH L11	PCIe Gen3 #12 / SATA #1		3h	PCIe Gen3 #12 (x4)		N/A		
CPU L0	PCIe Gen4 x4Lane 0	06h	0h	PCIe Gen4 (x4) L0	1x4 Lane Reversal Enabled	PCIE4_L3	06h	0h
CPU L1	PCIe Gen4 x4Lane 1			PCIe Gen4 (x4) L1		PCIE4_L2		
CPU L2	PCIe Gen4 x4Lane 2			PCIe Gen4 (x4) L2		PCIE4_L1		
CPU L3	PCIe Gen4 x4Lane 3			PCIe Gen4 (x4) L3		PCIE4_L0		

PCIe Port Assignment	
PCIE3_P1	(USB3_P1)
PCIE3_P2	(USB3_P2)
PCIE3_P3	WWAN Lane 1
PCIE3_P4	WWAN Lane 0
PCIE3_P5	(WLAN)
PCIE3_P6	(Reserved)
PCIE3_P7	(GbE PHY)
PCIE3_P8	(SD Card)
PCIE3_P9 (x4)	(dGPU)
PCIE4 (x4)	NVMe SSD

USB 3.1 Port Assignment	
USB3_P1	Type-A Port (DCI)
USB3_P2	Type-A Port (AOU)
USB3_P3	(PCIE3_P3)
USB3_P4	(PCIE3_P4)

USB 2.0 Port Assignment	
USB2_P1	Type-A Port (DCI)
USB2_P2	WWAN
USB2_P3	Fingerprint Reader
USB2_P4	RGB / IR Hybrid Camera
USB2_P5	Type-C Port B
USB2_P6	Type-C Port C
USB2_P7	Type-A Port (AOU)
USB2_P8	(Touch Panel)
USB2_P9	(Smart Card Reader)
USB2_P10	(Bluetooth)

SATA Port Assignment	
SATA_P0	(PCIE3_P11)
SATA_P1	(PCIE3_P12)



PCIECLK and CLKREQ# Port Assignment		
Port 0	PCle Gen4 (x4)	NVMe SSD
Port 1	PCle Gen3 P5	(M.2 WLAN)
Port 2	PCle Gen3 P1	M.2 WWAN
Port 3	PCle Gen3 P9 (x4)	(dGPU)
Port 4	PCle Gen3 P7	(GbE PHY)
Port 5	PCle Gen3 P8	(SD Card)
Port 6	PCle Gen3 P6	(Reserved)

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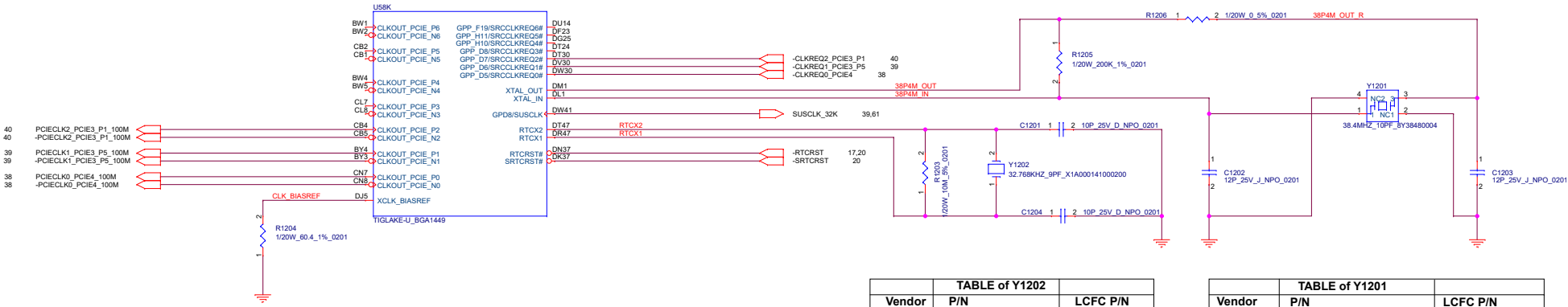
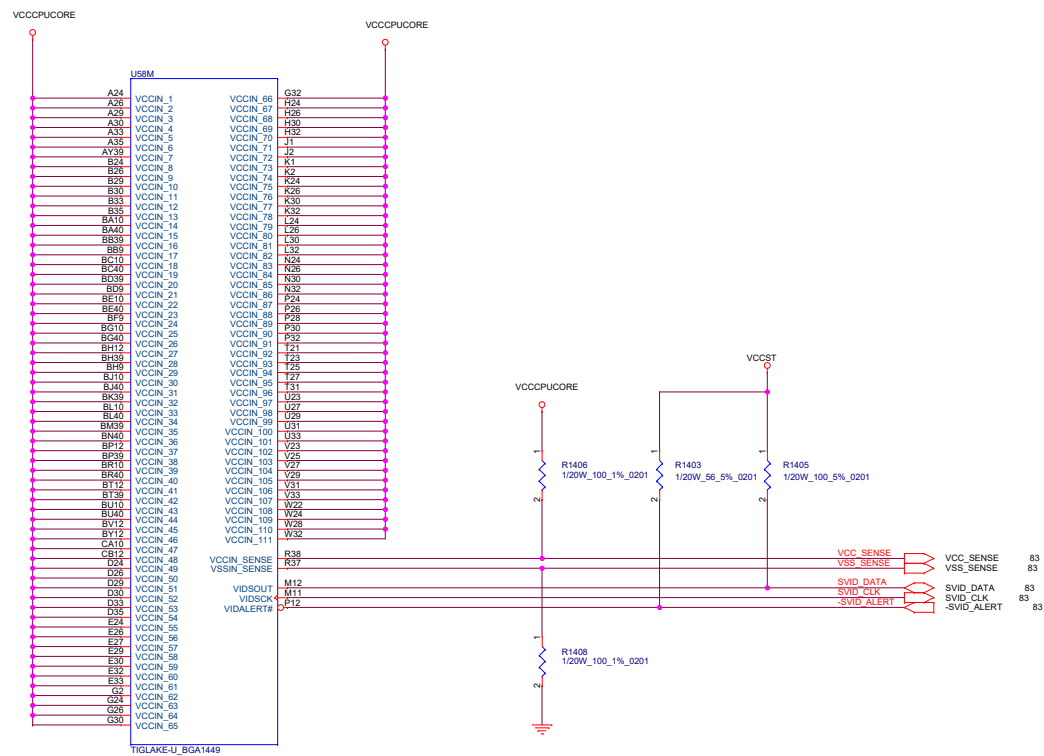
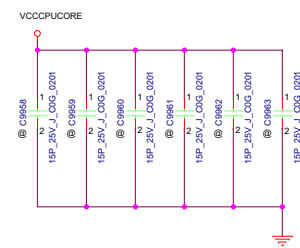
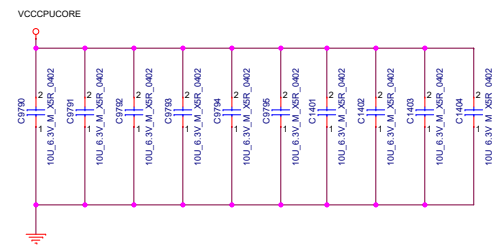
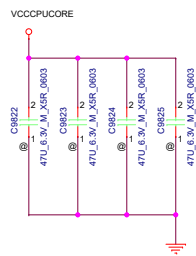
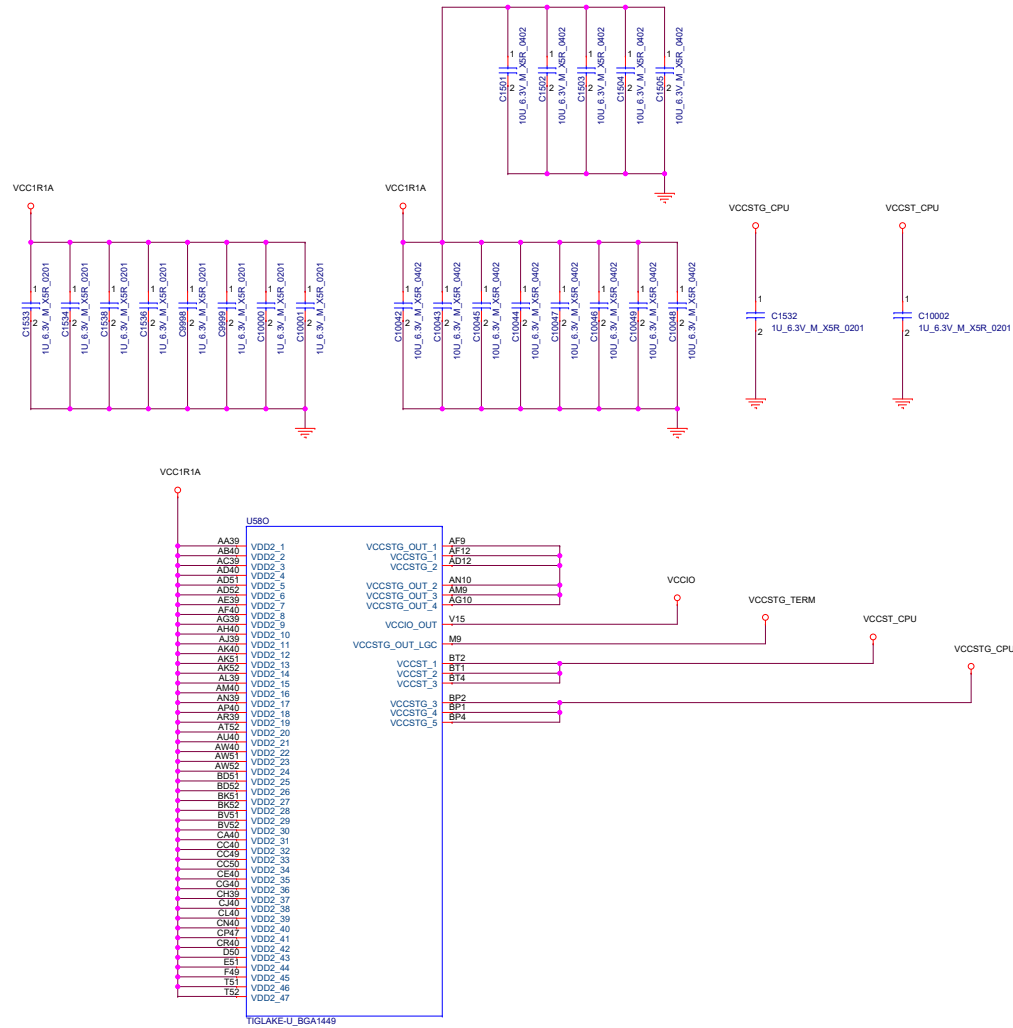
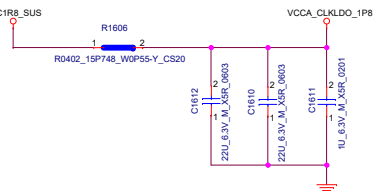
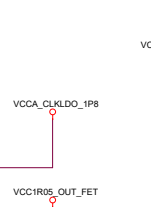
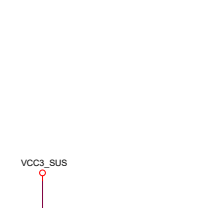
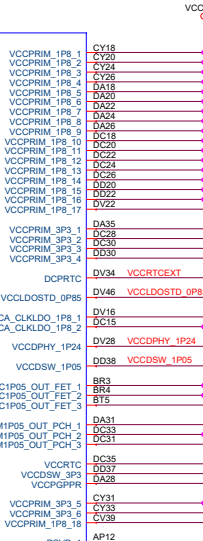
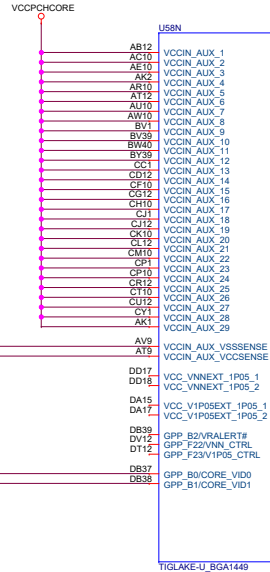
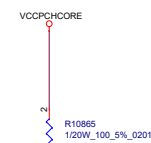
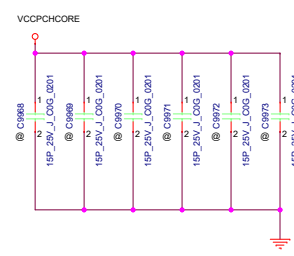
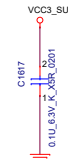
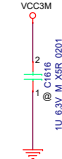
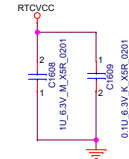
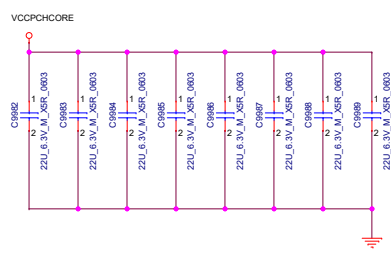
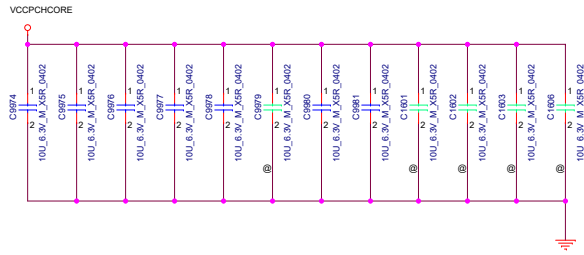


TABLE of Y1202		
Vendor	P/N	LCFC P/N
EPSON	X1A000141000200	SJ10000IX00
TXC	9H03280012	SJ10000J900
KDS	1TJF090DJ1A000B	SJ100069400

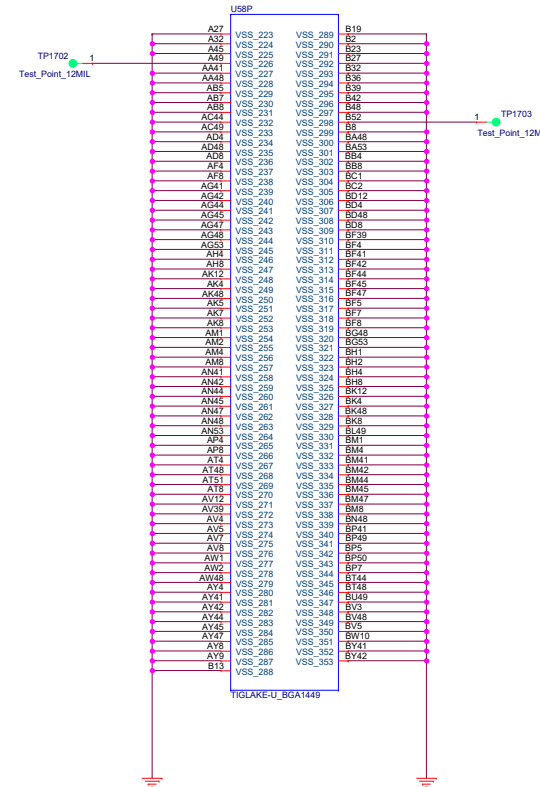
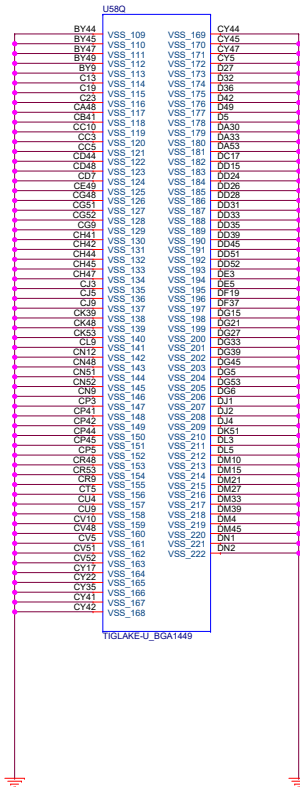
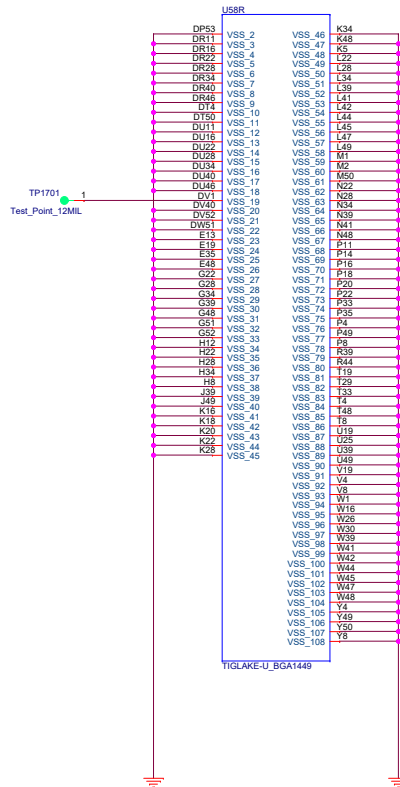
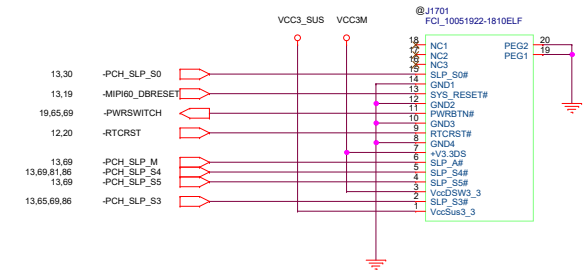
TABLE of Y1201		
Vendor	P/N	LCFC P/N
TXC	8Y38480004	SJ10000SN00
KDS	7AF03840A04	
MURATA	XRCGB38M4000F2P17R0	







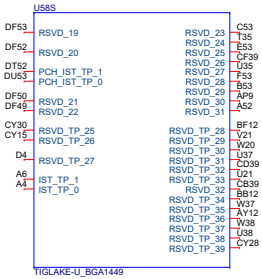
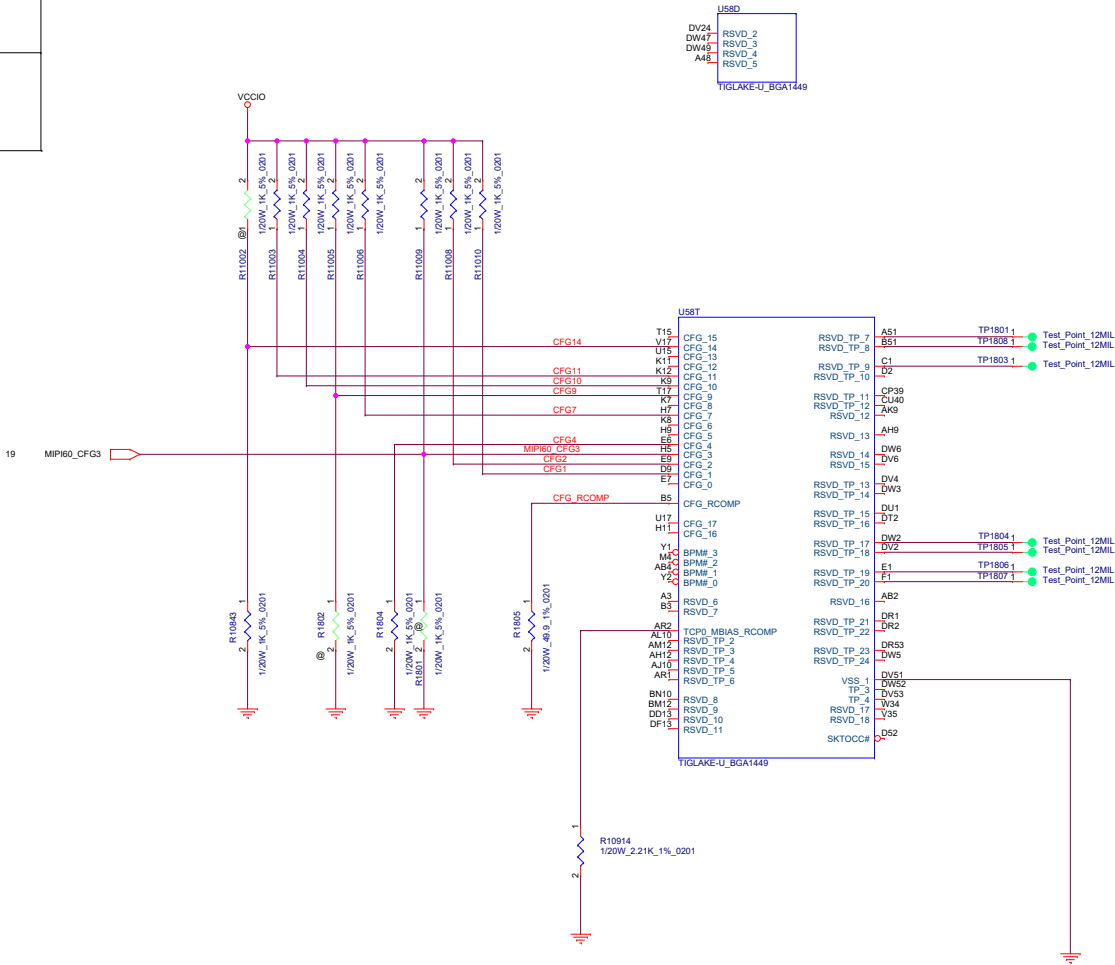
APS/PETS Interface

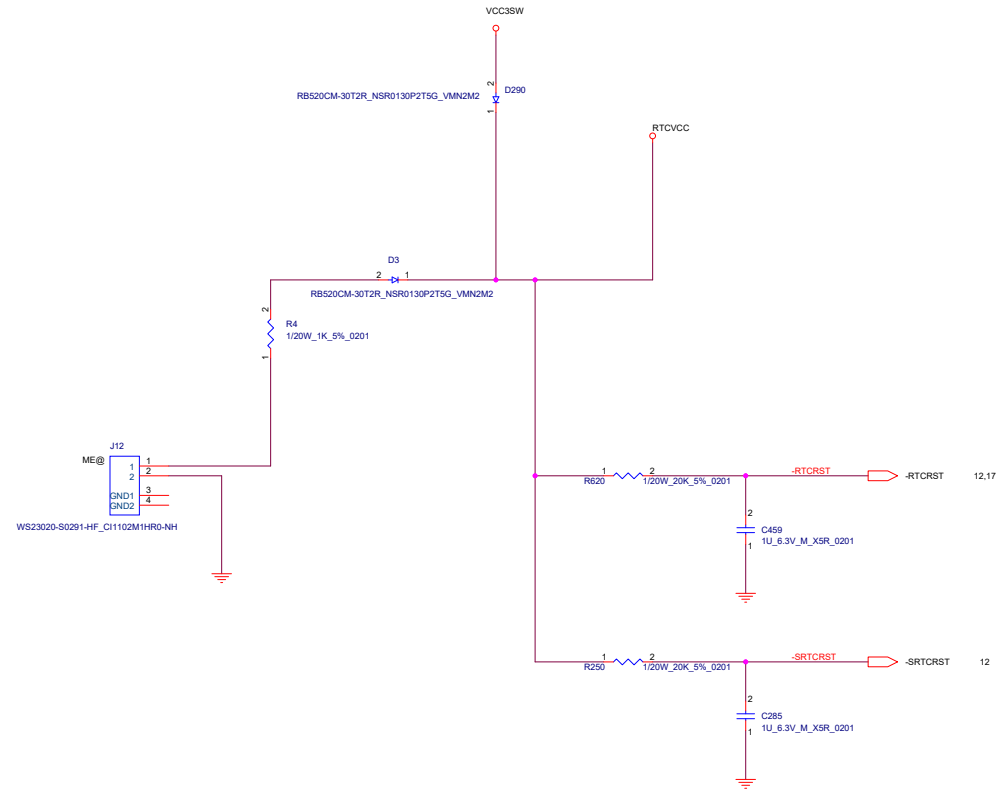


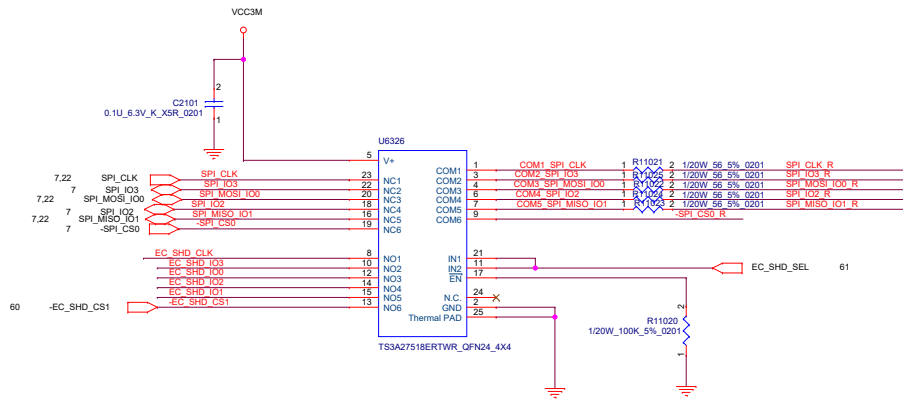
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TABLE

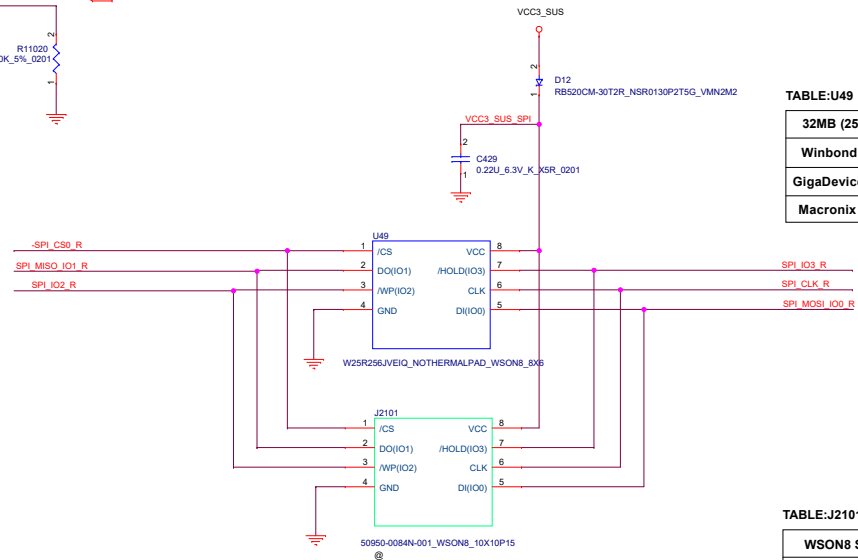
CFG3: MSR Privacy Bit Feature
1: MSR (C80h) bit[0] setting
0: MSR (C80h) bit[0] overridden
CFG4: eDP Enable
1:Disabled
0:Enabled
CFG9: SVID Bus Communication
1:Enabled
0:Disabled
CFG14: PEG60 Lane Reversal
1:Normal
0:Reversed





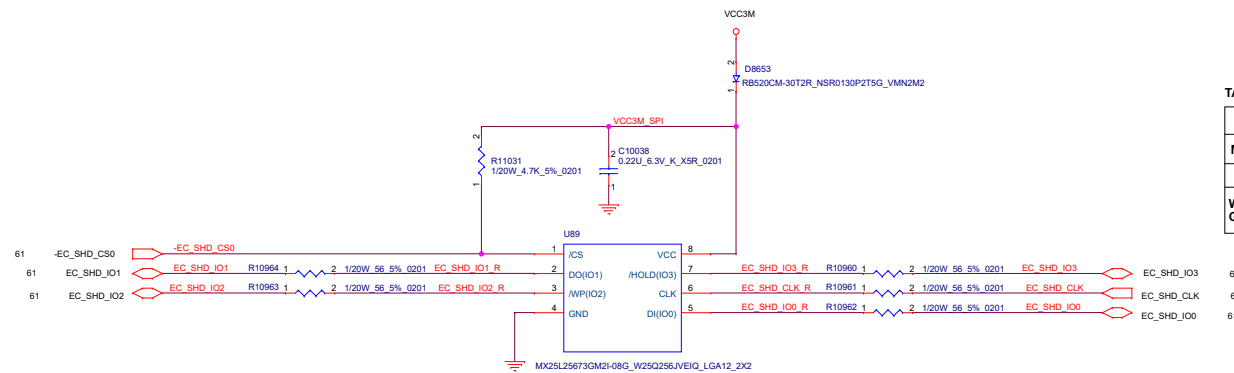


1	VCC	D12.1	GND	GND	2
3	CS#	R322.2	R681.2	CLK	4
5	MISO	R694.2	R674.2	MOSI	6
7	(KEY)	N/A	N/A	(RESET)	8



32MB (256Mb) 8x6mm WSON8	
Winbond	W25R256JVEIQ
GigaDevice	GD25R256DYIGR
Macronix	MX77L25650FZ4142

WSON8 SPI FLASH SOCKET	
ACES	50950-0084N-001
DediProg	SOK-SPI-WSON68



32MB (256Mb) 200MIL SOIC8	
MACRONIX	MX25L25673GM21-08G
32MB (256Mb) 8x6mm WSON8	
WINBOND GIGADEVICE	W25Q256JVEIQ GD25B256DYIGR

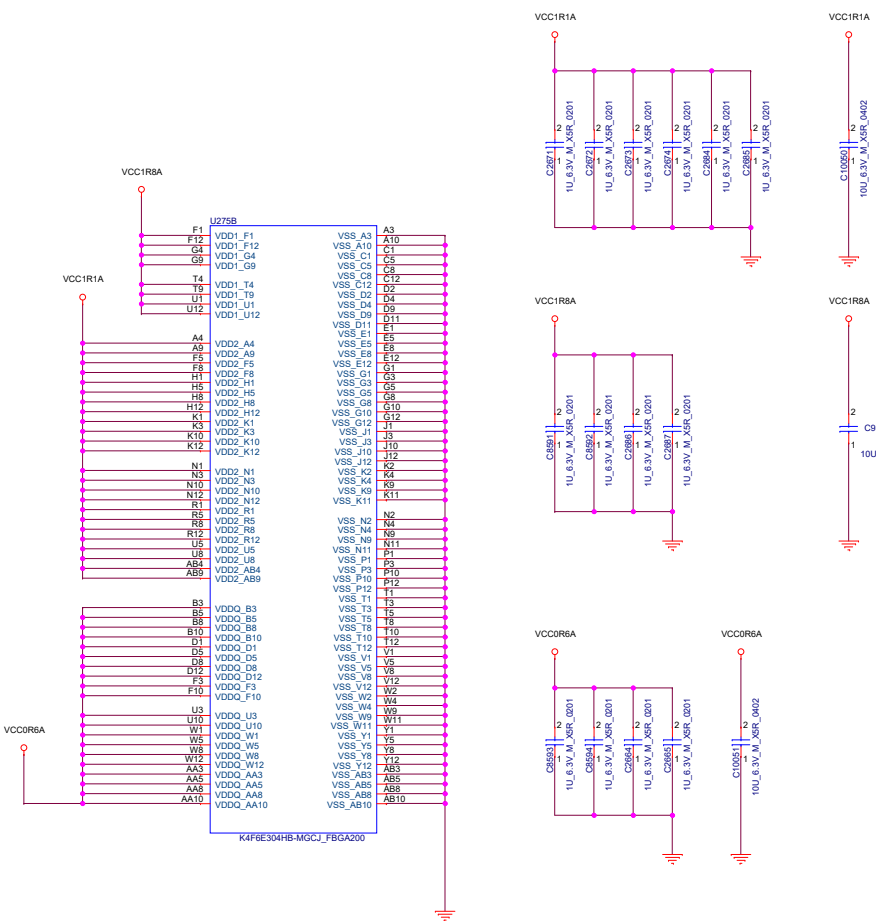
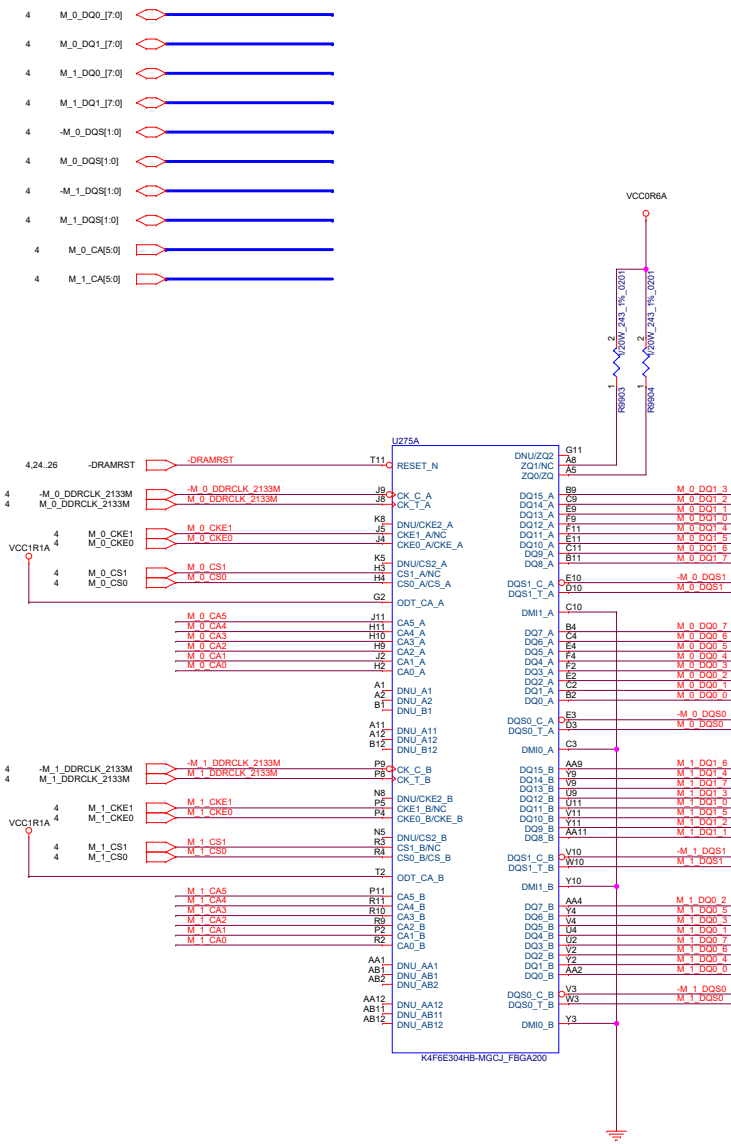


TABLE : LPDDR4x Source

Supplier	Capacity	Supplier's P/N	Package Size		Die	Device Configuration	Memory
SK Hynix	16Gb	H9HCNNNBKMLXR-NEE	10.0 x 15.0 mm	DDP	8Gb (512Mx16x1Ch)	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gb	H9HCNNNPCMLXR-NEE	10.0 x 15.0 mm	QDP	8Gb (512Mx16x1Ch)	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gb	H9HCNNNFAMMLXR-NEE	10.0 x 15.0 mm	ODP	8Gb (1Gx8x1Ch)	2 Rank x (1Gx16) x 2 Ch	32GB
Samsung	16Gb	K4U6E3S4AA-MGCR	10.0 x 15.0 mm	SDP	16Gb (512Mx16x2Ch)	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gb	K4UBE3D4AA-MGCR	10.0 x 15.0 mm	DDP	16Gb (512Mx16x2Ch)	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gb	K4UCE3Q4AA-MGCR	10.0 x 15.0 mm	QDP	16Gb (T.B.D)	2 Rank x (1Gx16) x 2 Ch	32GB
Micron	16Gb	MT53E512M32D2NP-046 WT:E	10.0 x 14.5 mm	DDP	8Gb (512Mx16x1Ch)	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gb	MT53E1G32D2NP-046 WT:A	10.0 x 14.5 mm	DDP	16Gb (T.B.D)	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gb	MT53E2G32D4NQ-046 WT:A	10.0 x 14.5 mm	QDP	16Gb (T.B.D)	2 Rank x (1Gx16) x 2 Ch	32GB

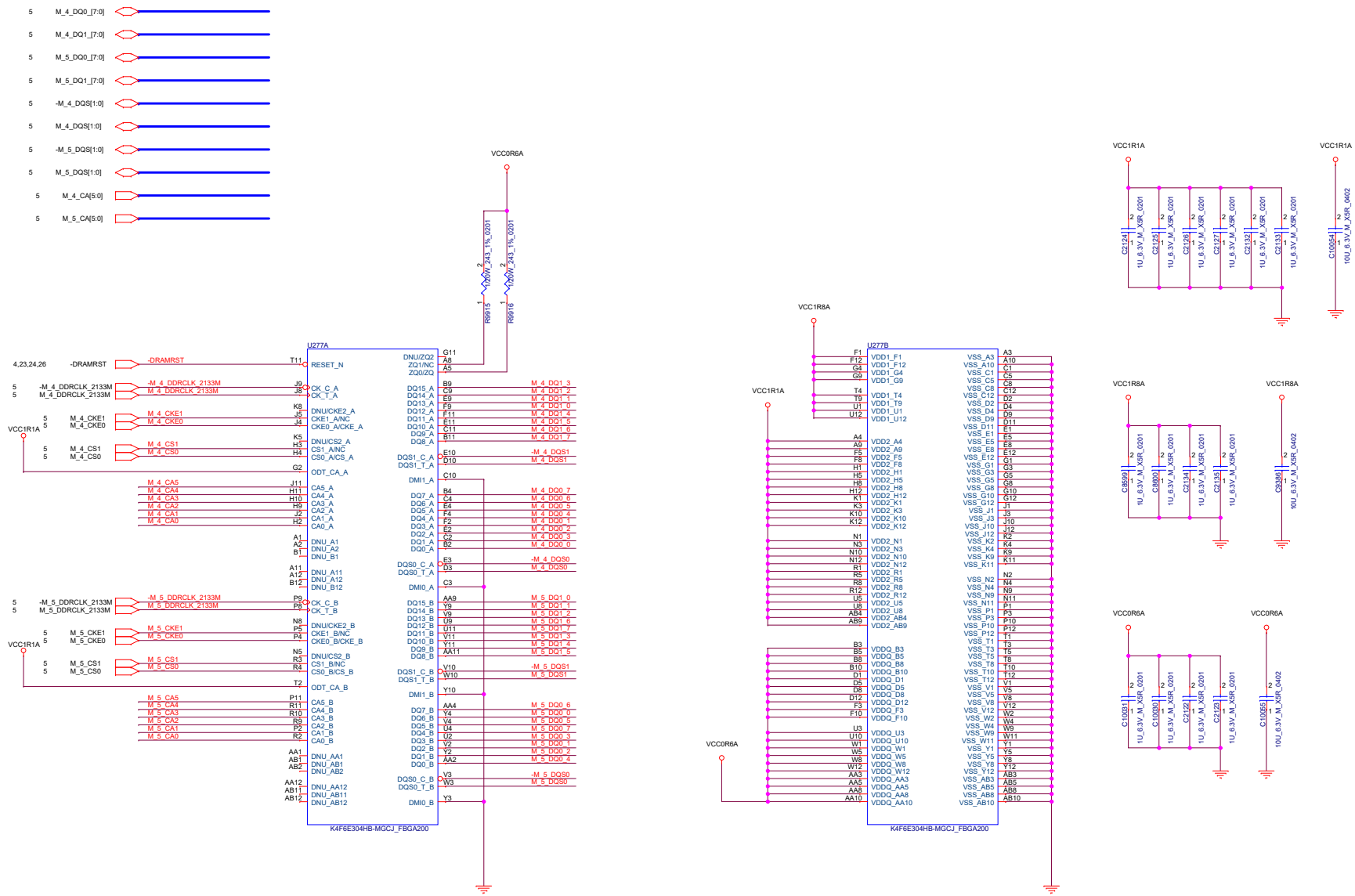
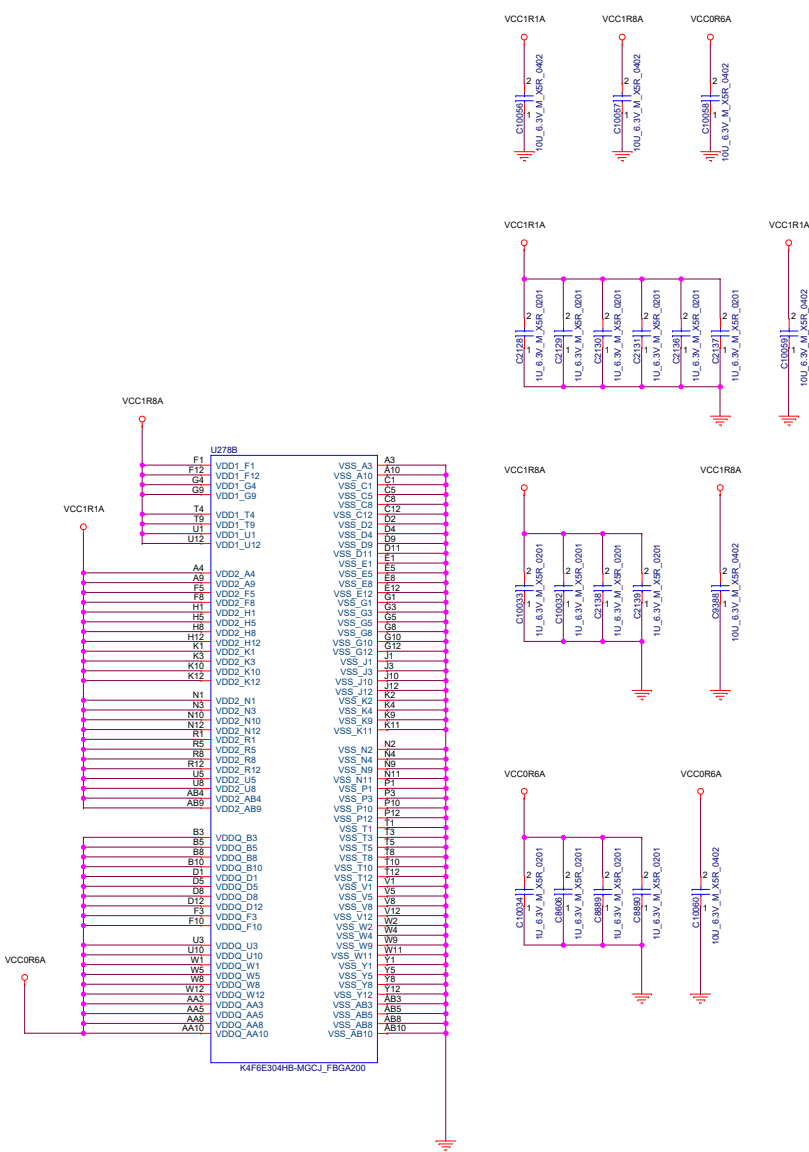
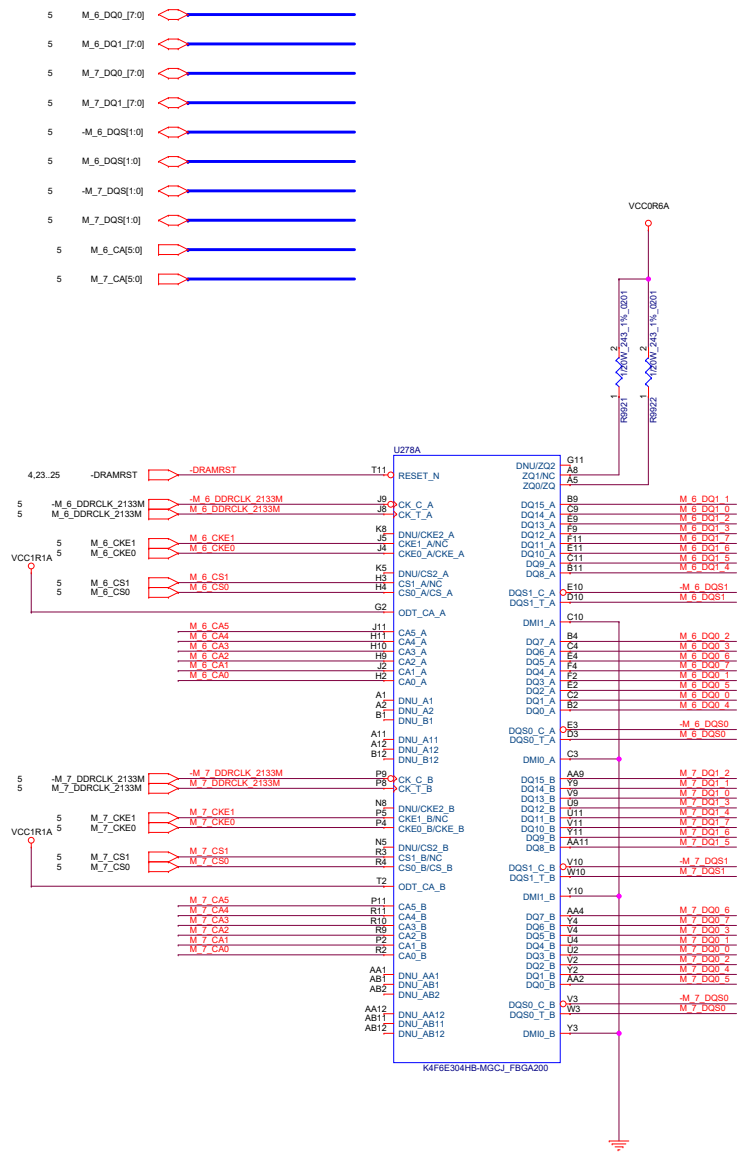


TABLE : LPDDR4x Source

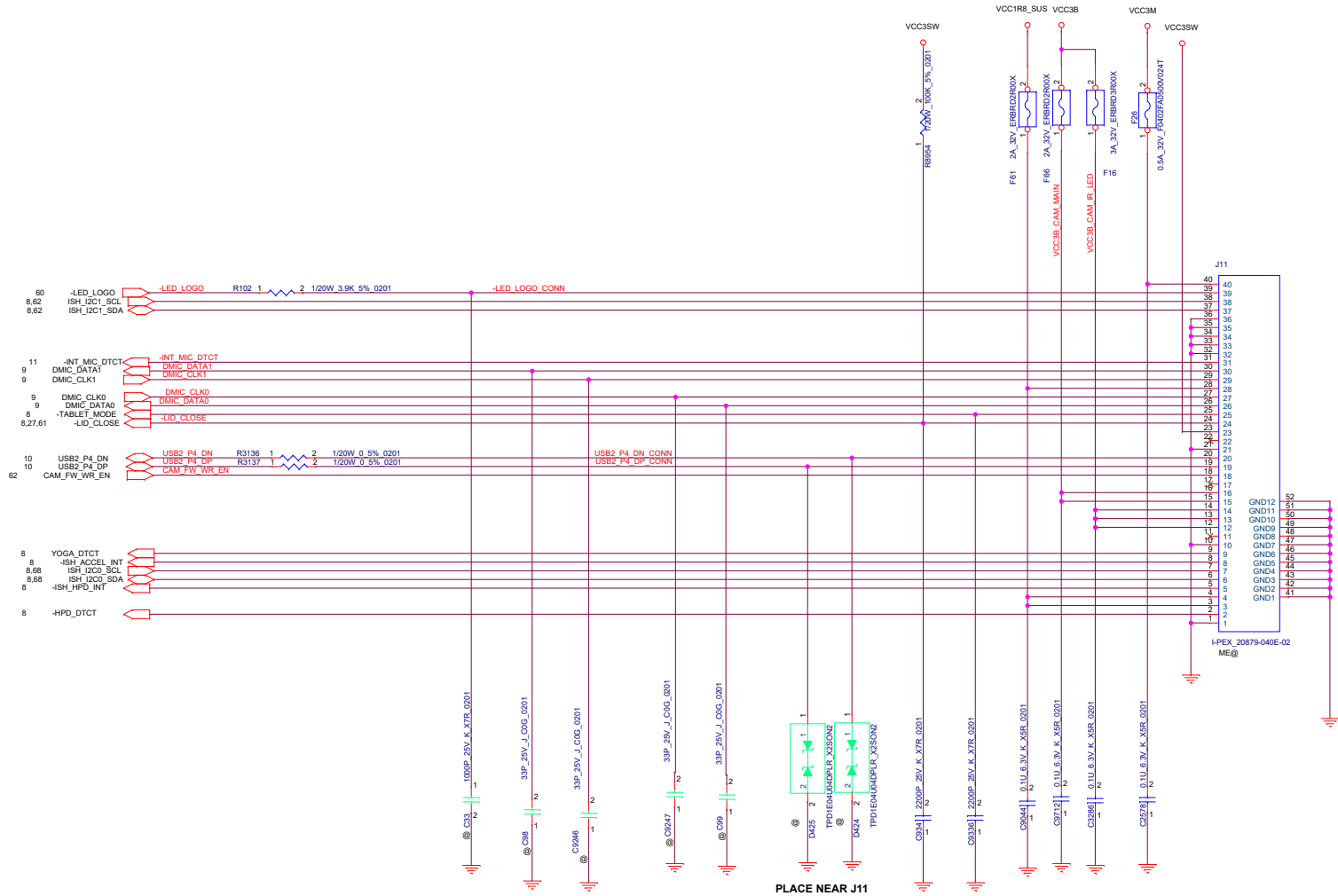
Supplier	Capacity	Supplier's P/N	Package Size		Die	Device Configuration	Memory
SK Hynix	16Gb	H9HCNNNBKMLXR-NEE	10.0 x 15.0 mm	DDP	8Gb (512Mx16x1Ch)	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gb	H9HCNNNCPMMLXR-NEE	10.0 x 15.0 mm	QDP	8Gb (512Mx16x1Ch)	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gb	H9HCNNNFAMMLXR-NEE	10.0 x 15.0 mm	ODP	8Gb (1Gx8x1Ch)	2 Rank x (1Gx16) x 2 Ch	32GB
Samsung	16Gb	K4UE6S34AA-MGCR	10.0 x 15.0 mm	SDP	16Gb (512Mx16x2Ch)	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gb	K4UBE3D4AA-MGCR	10.0 x 15.0 mm	DDP	16Gb (512Mx16x2Ch)	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gb	K4UCE3Q4AA-MGCR	10.0 x 15.0 mm	QDP	16Gb (T.B.D)	2 Rank x (1Gx16) x 2 Ch	32GB
Micron	16Gb	MT53E512M32D2NP-046 WT:E	10.0 x 14.5 mm	DDP	8Gb (512Mx16x1Ch)	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gb	MT53E1G32D2NP-046 WT:A	10.0 x 14.5 mm	DDP	16Gb (T.B.D)	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gb	MT53E2G32D4NQ-046 WT:A	10.0 x 14.5 mm	QDP	16Gb (T.B.D)	2 Rank x (1Gx16) x 2 Ch	32GB



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TABLE : LPDDR4x Source

Supplier	Capacity	Supplier's P/N	Package Size	Die	Device Configuration	Memory
SK Hynix	16Gb	H9HCNNNBKMLXR-NEE	10.0 x 15.0 mm	DDP	8Gb (512Mx16x1Ch)	1 Rank x (512Mx16) x 2 Ch
	32Gb	H9HCNNNCPMMLXR-NEE	10.0 x 15.0 mm	QDP	8Gb (512Mx16x1Ch)	2 Rank x (512Mx16) x 2 Ch
	64Gb	H9HCNNNFAMMLXR-NEE	10.0 x 15.0 mm	ODP	8Gb (1Gx8x1Ch)	2 Rank x (1Gx16) x 2 Ch
Samsung	16Gb	K4U6E3S4AA-MGCR	10.0 x 15.0 mm	SDP	16Gb (512Mx16x2Ch)	1 Rank x (512Mx16) x 2 Ch
	32Gb	K4UBE3D4AA-MGCR	10.0 x 15.0 mm	DDP	16Gb (512Mx16x2Ch)	2 Rank x (512Mx16) x 2 Ch
	64Gb	K4UCE3Q4AA-MGCR	10.0 x 15.0 mm	QDP	16Gb (1Gx8x1Ch)	2 Rank x (1Gx16) x 2 Ch
Micron	16Gb	MT53E12M32D2NP-046 WT:E	10.0 x 14.5 mm	DDP	8Gb (512Mx16x1Ch)	1 Rank x (512Mx16) x 2 Ch
	32Gb	MT53E1G32D2NP-046 WT:A	10.0 x 14.5 mm	DDP	16Gb (T.B.D)	2 Rank x (512Mx16) x 2 Ch
	64Gb	MT53E2G32D4NQ-046 WT:A	10.0 x 14.5 mm	QDP	16Gb (T.B.D)	2 Rank x (1Gx16) x 2 Ch



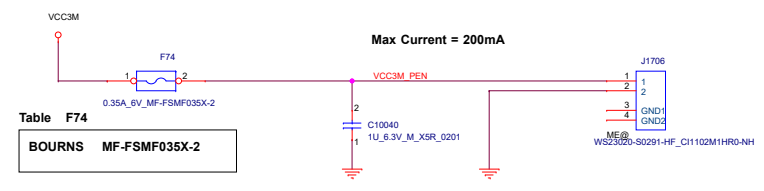
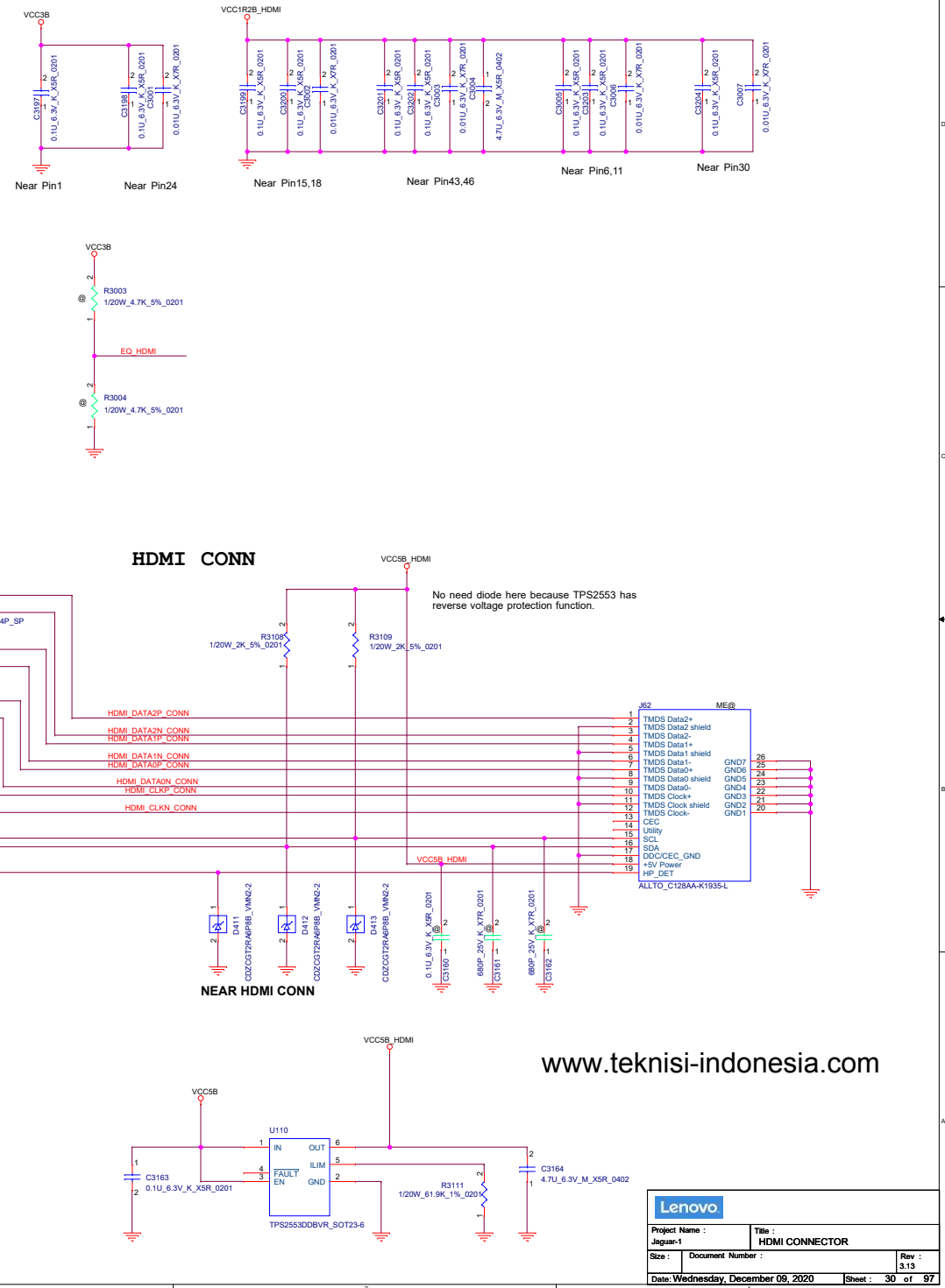
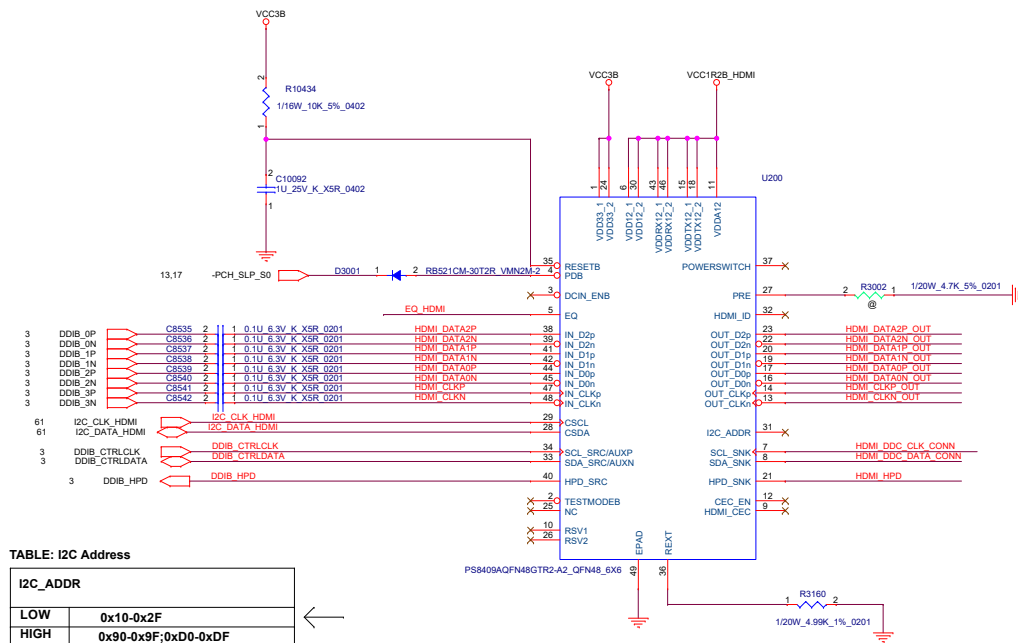
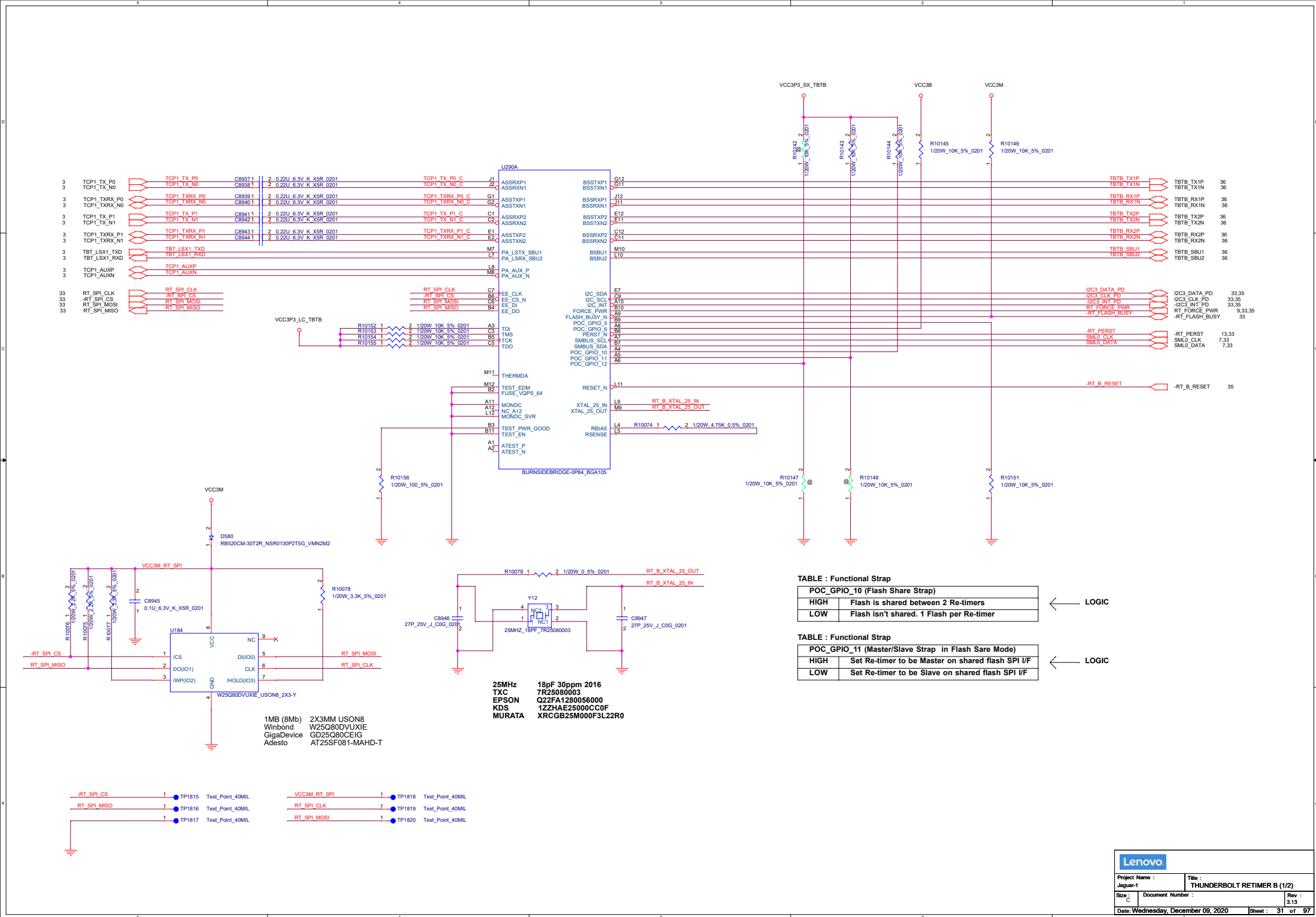
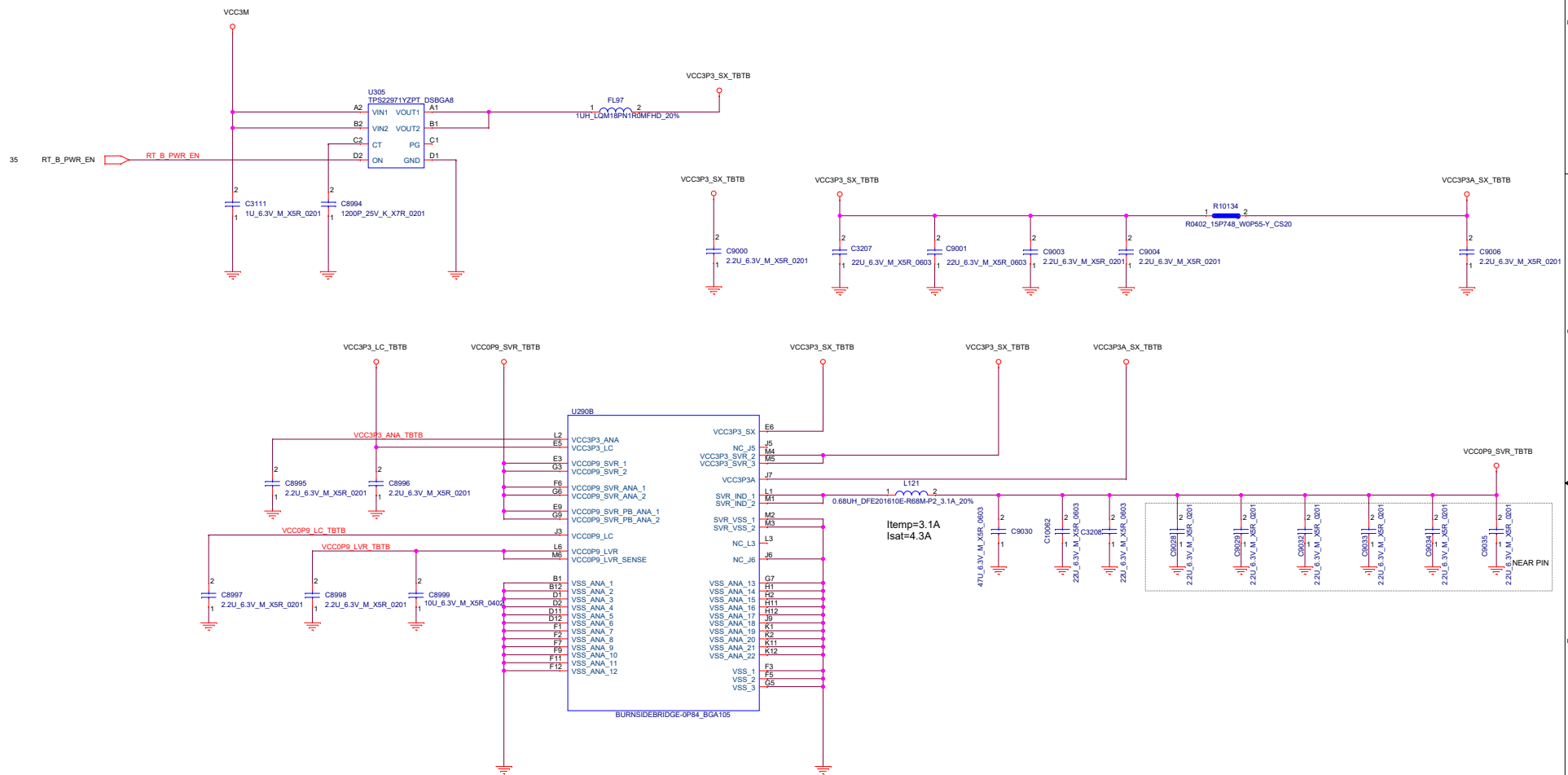


Table F74

BOURNS	MF-FSMF035X-2
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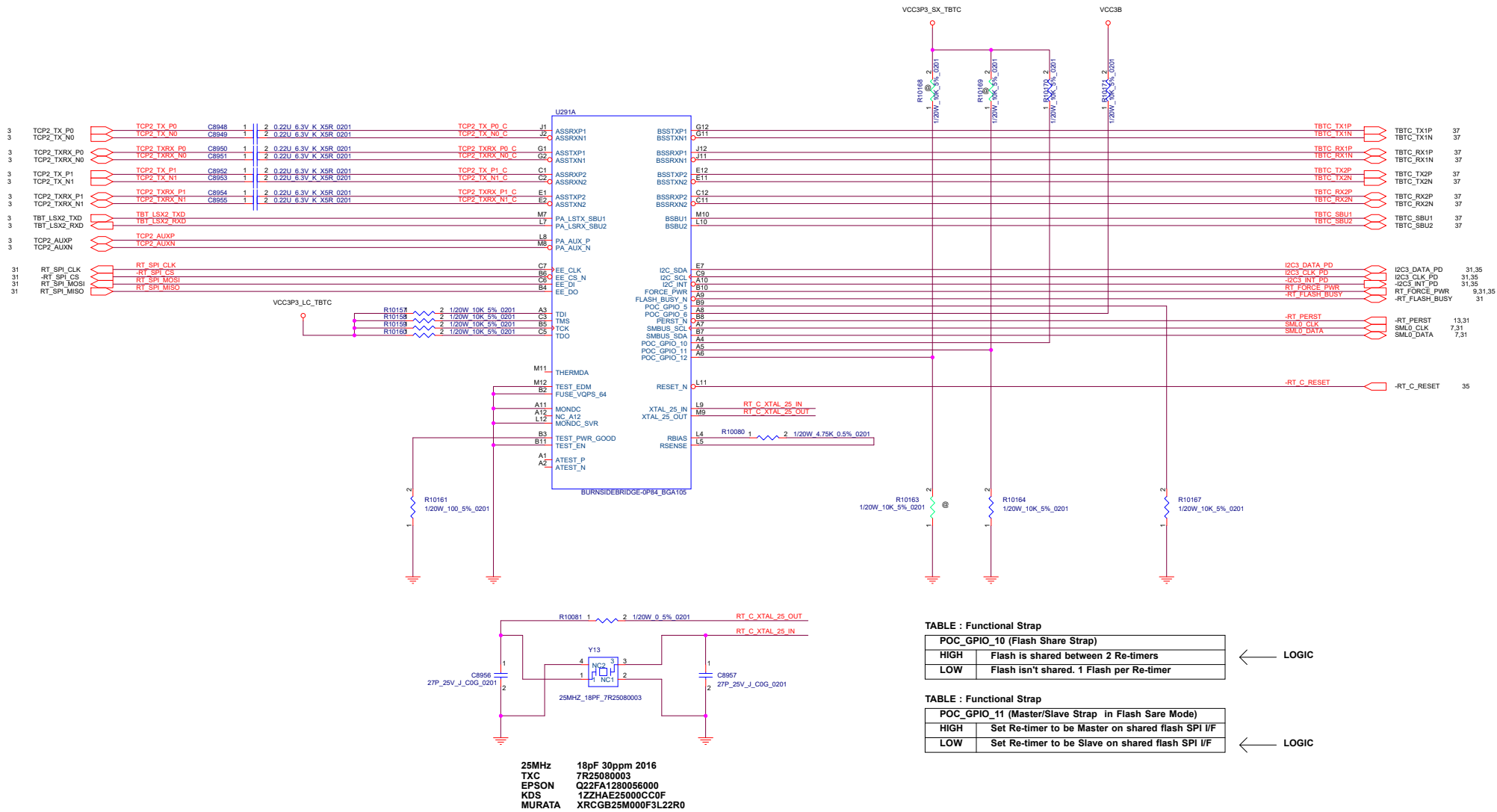


TABLE : Functional Strap

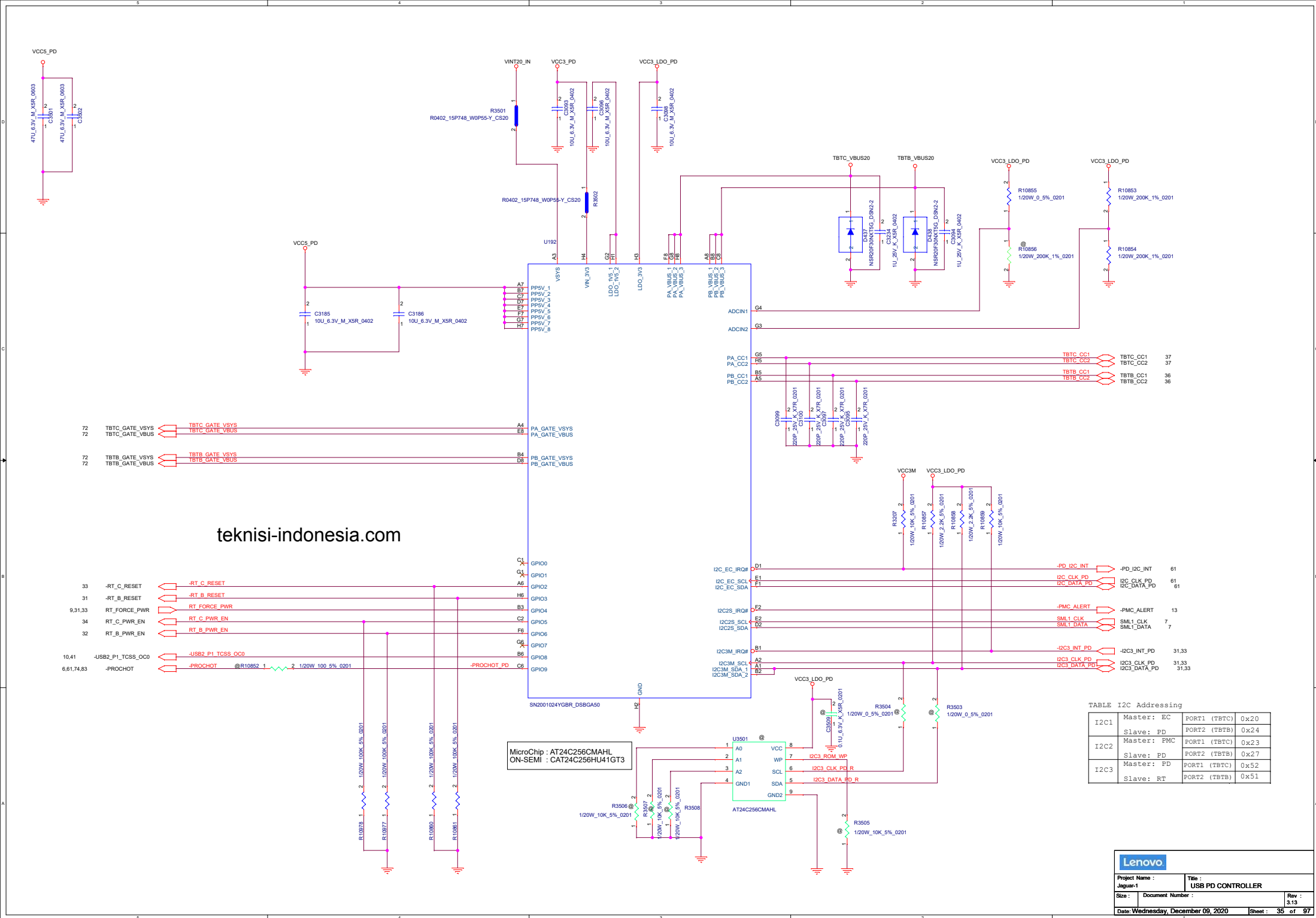
POC_GPIO_10 (Flash Share Strap)	
HIGH	Flash is shared between 2 Re-timers
LOW	Flash isn't shared. 1 Flash per Re-timer

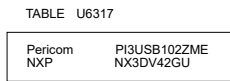
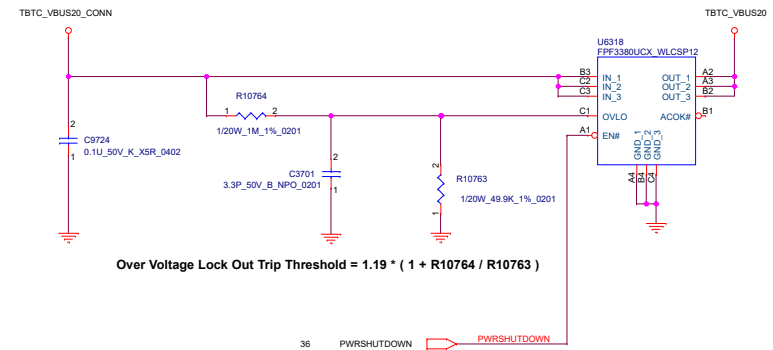
← LOGIC

TABLE : Functional Strap

POC_GPIO_11 (Master/Slave Strap in Flash Share Mode)	
HIGH	Set Re-timer to be Master on shared flash SPI I/F
LOW	Set Re-timer to be Slave on shared flash SPI I/F

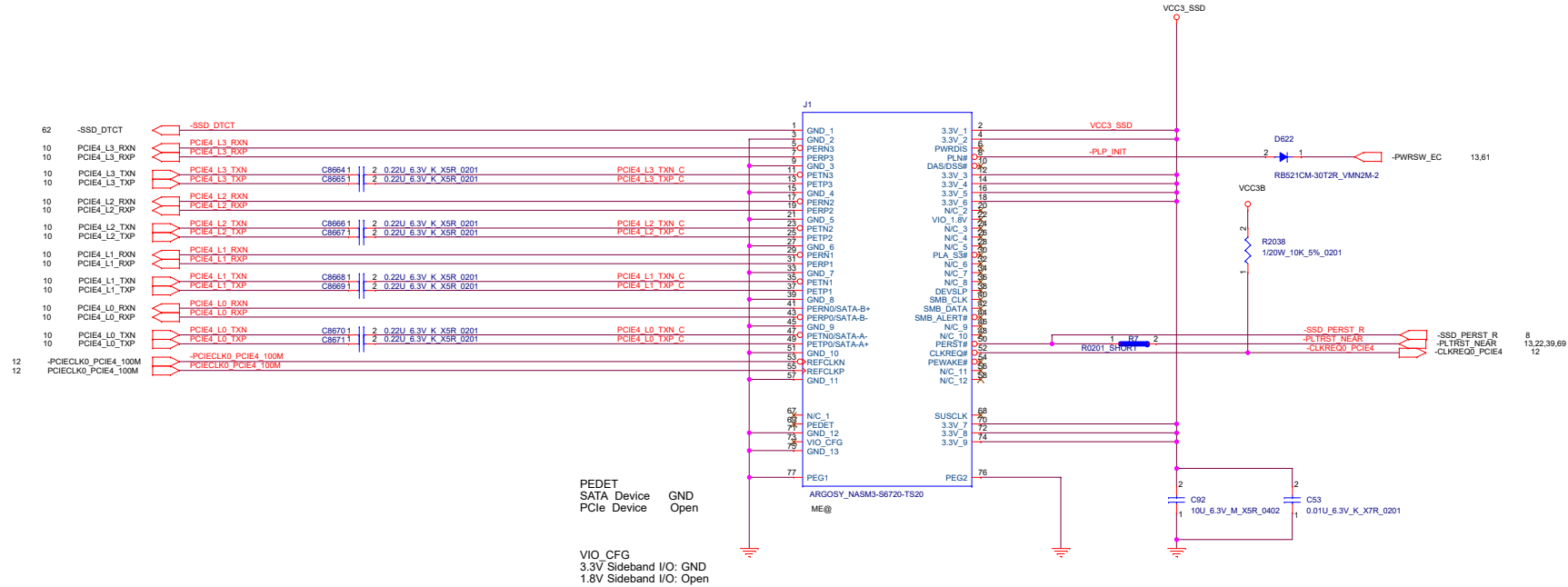
← LOGIC



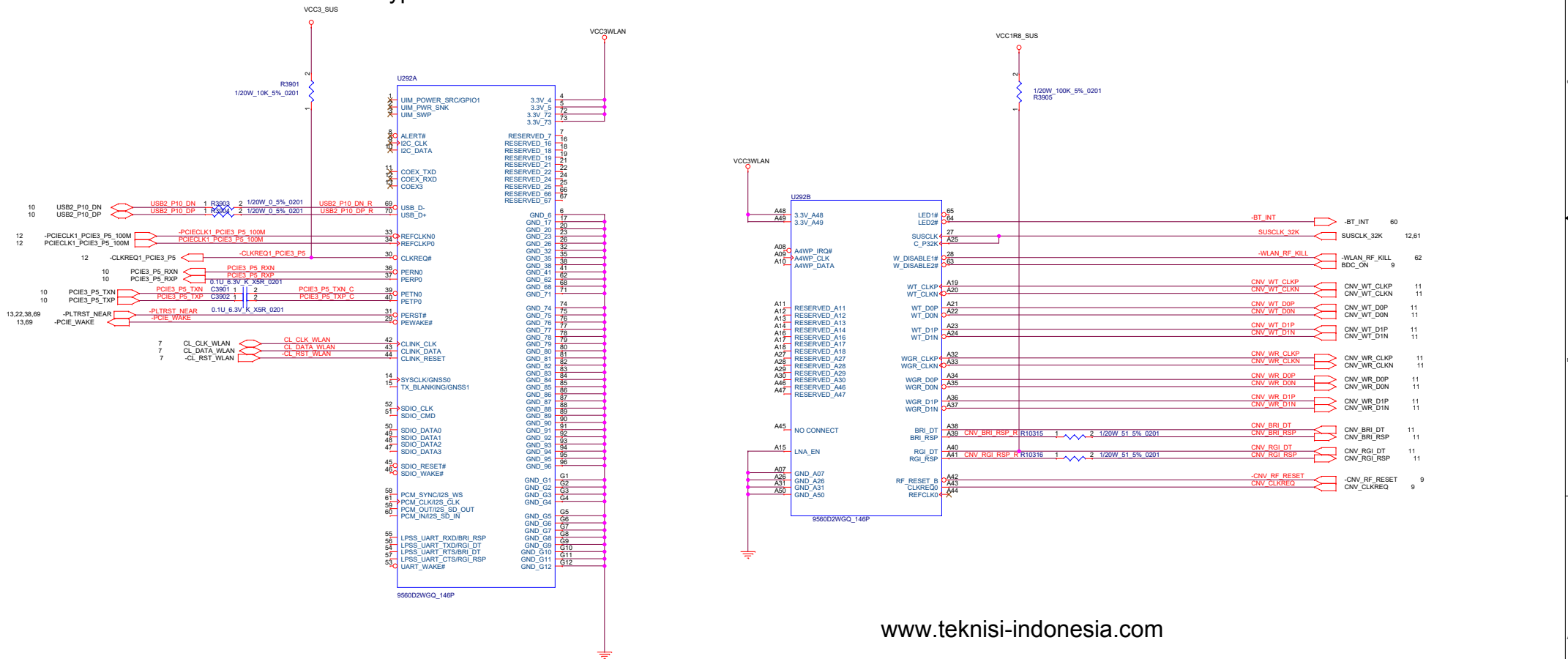


M.2 Socket 3 (Key-M) for 2280 S3 SSD

H=2.00mm Connector



M.2 Type 1216 Module for WLAN / Bluetooth



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M.2 Socket 2 (Key-B) for WWAN 3G/4G: 3042 S3 5G: 3042 S3 H=2.00mm Connector

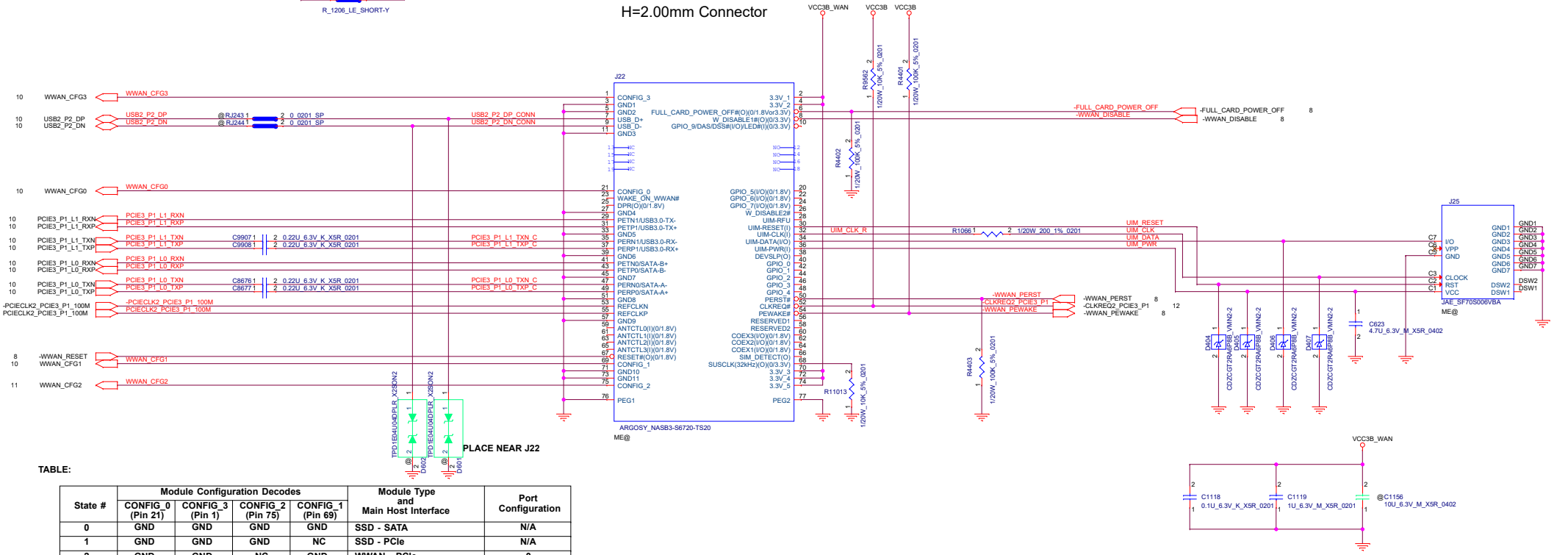
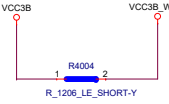
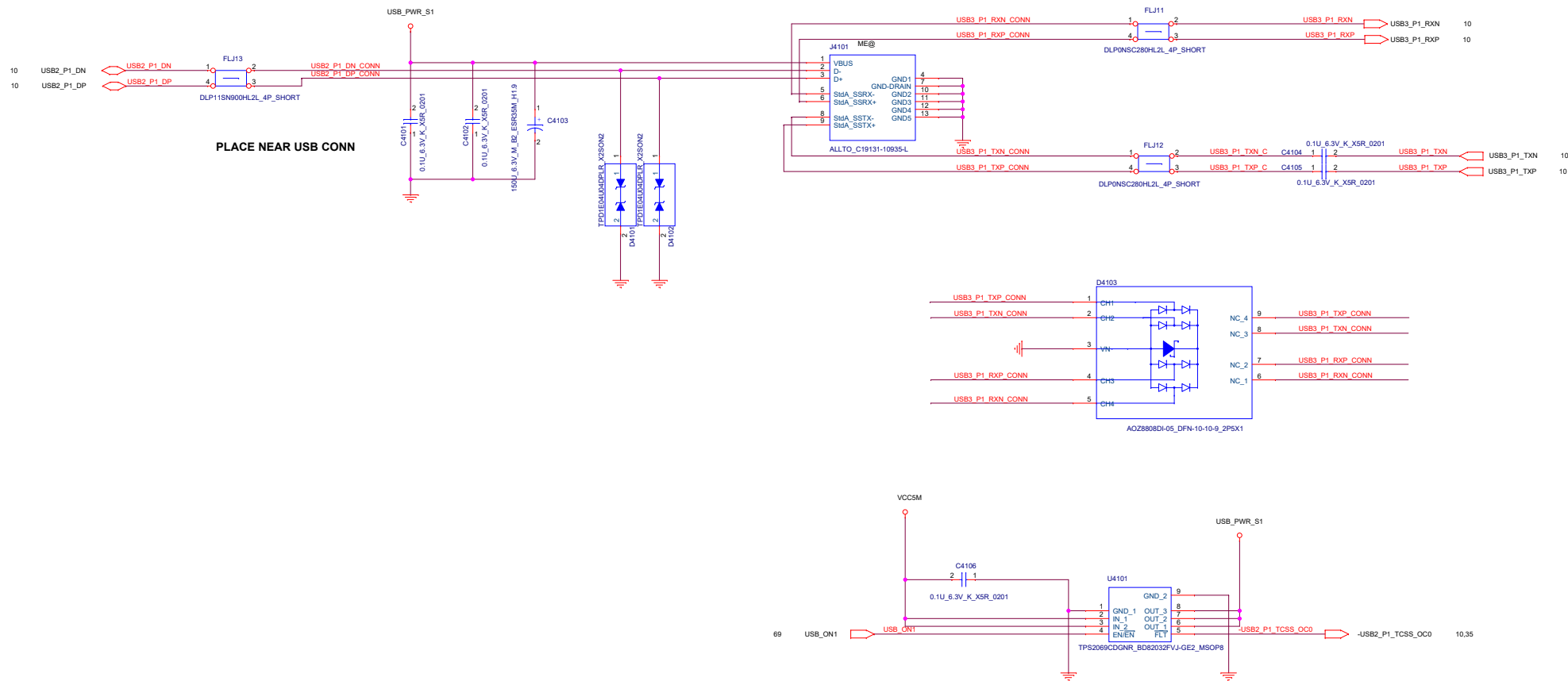



TABLE:

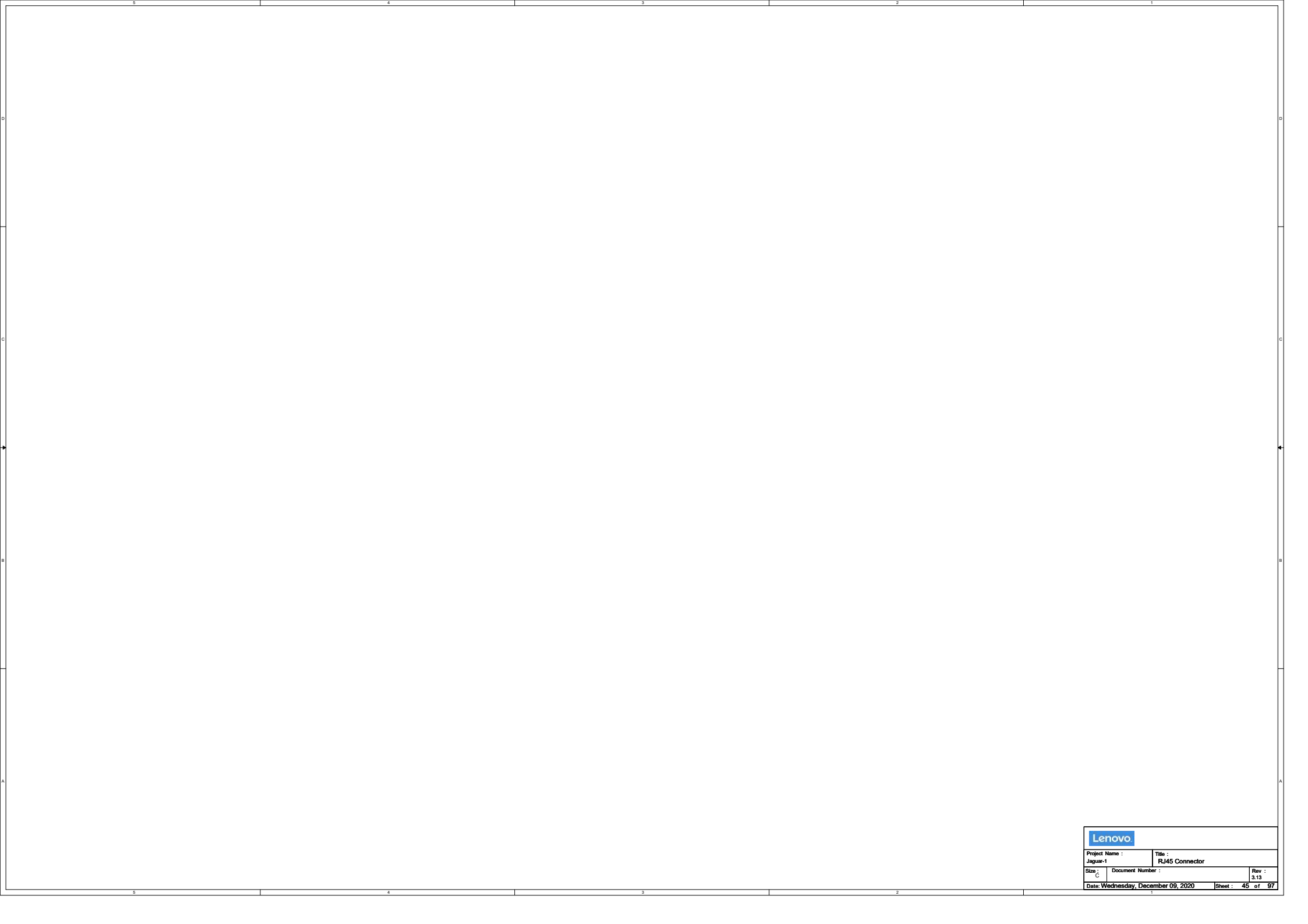
State #	Module Configuration Decodes				Module Type and Main Host Interface	Port Configuration
	CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)		
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	GND	GND	NC	SSD - PCIe	N/A
2	GND	GND	NC	GND	WWAN - PCIe	0
3	GND	GND	NC	NC	WWAN - PCIe	1
4	GND	NC	GND	GND	WWAN - PCIe, USB 3.1 Gen1	0
5	GND	NC	GND	NC	WWAN - PCIe, USB 3.1 Gen1	1
6	GND	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	2
7	GND	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	3
8	NC	GND	GND	GND	WWAN - SSIC	0
9	NC	GND	GND	NC	WWAN - SSIC	1
10	NC	GND	NC	GND	WWAN - SSIC	2
11	NC	GND	NC	NC	WWAN - SSIC	3
12	NC	NC	GND	GND	WWAN - PCIe	2
13	NC	NC	GND	NC	WWAN - PCIe	3
14	NC	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	Vendor Defined
15	NC	NC	NC	NC	No Module Present	N/A



Sheet : 42 of 97

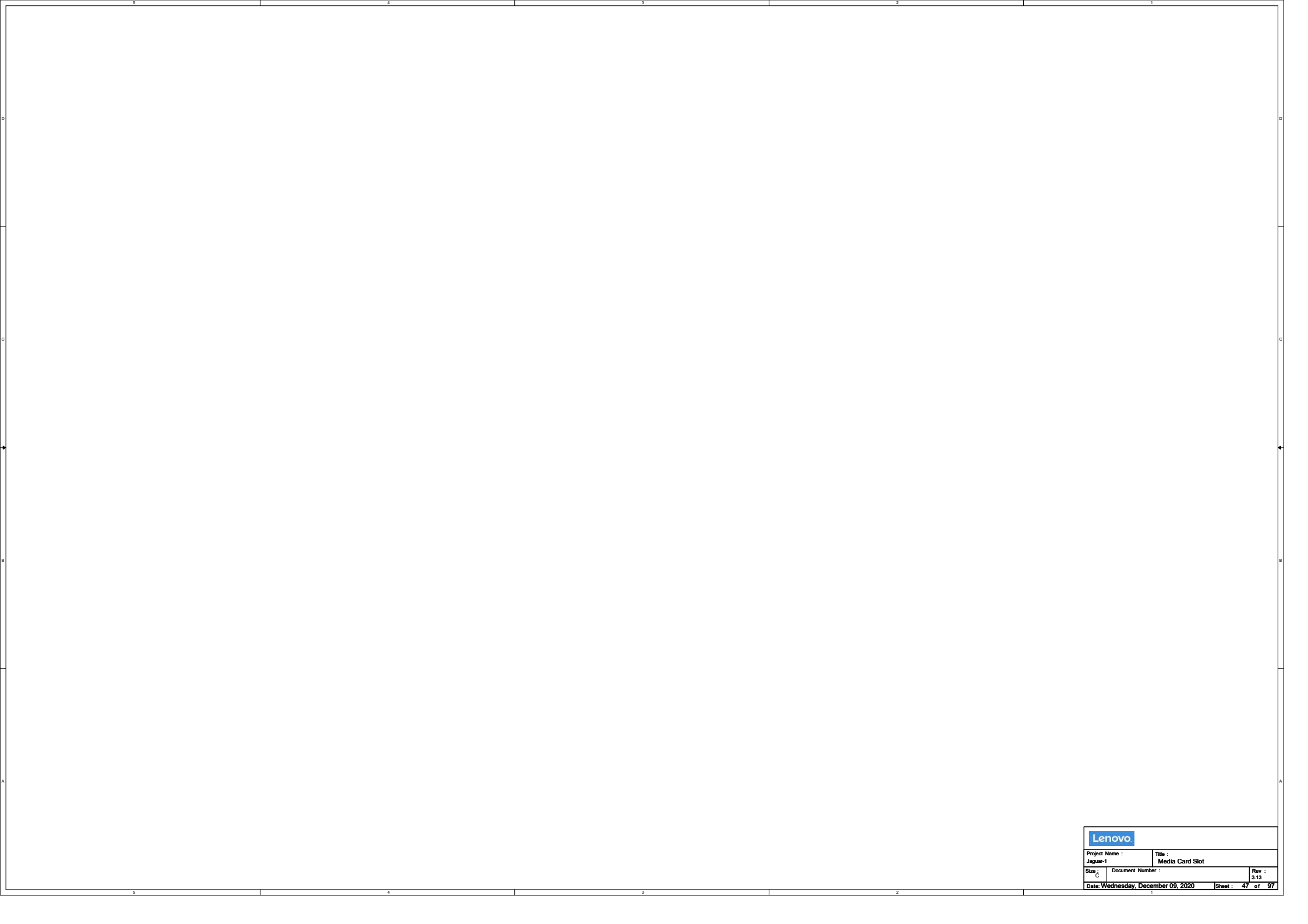
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Project Name : Jaguar-1		Title : BLANK
Size : C	Document Number :	Rev : 3.13
Date: Wednesday, December 09, 2020		Sheet : 43 of 97



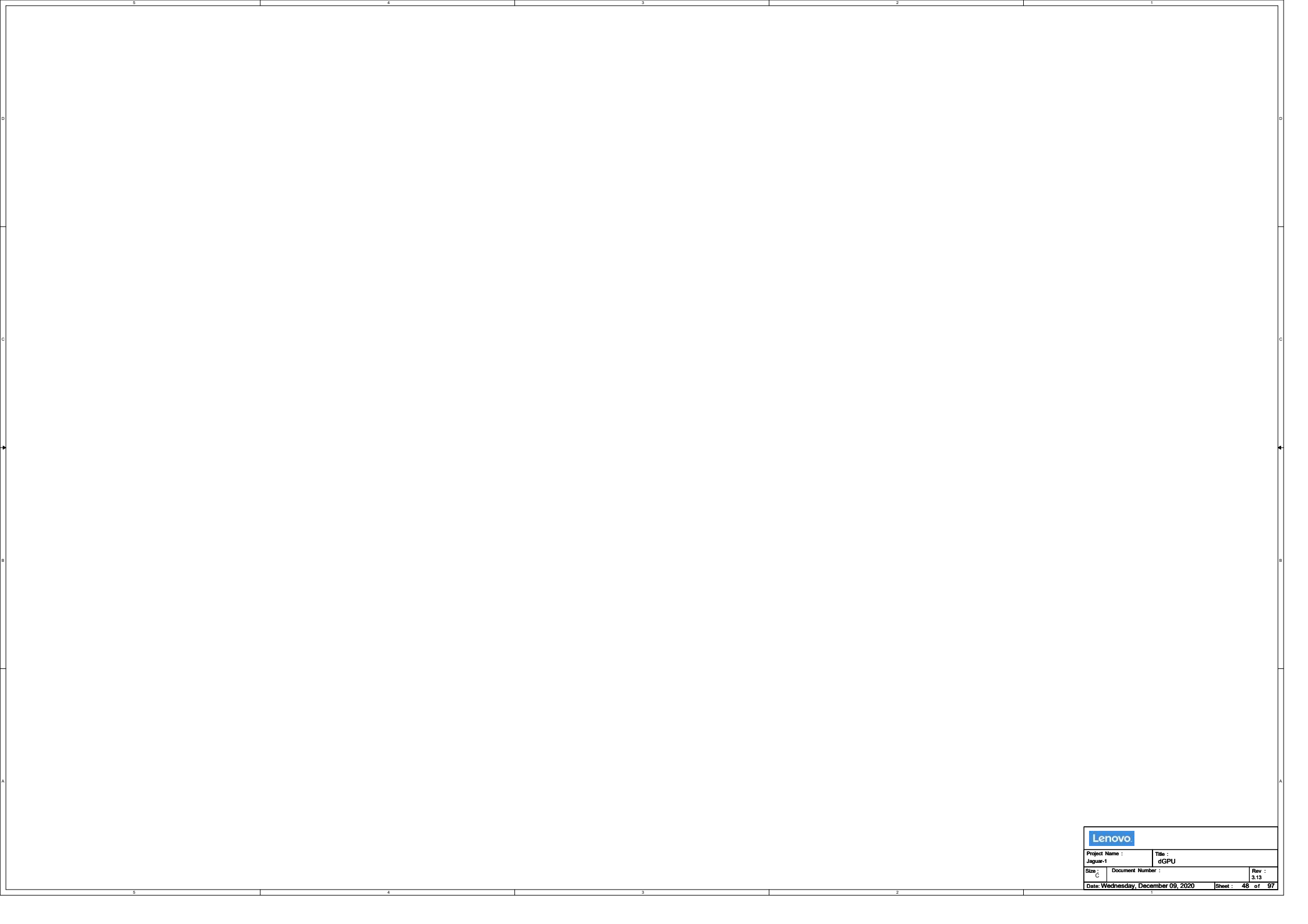
Lenovo

Project Name : Jaguar-1		Title : RJ45 Connector	
Size : C	Document Number :		Rev : 3.13
Date: Wednesday, December 09, 2020		Sheet : 45 of 97	



Lenovo

Project Name : Jaguar-1		Title : Media Card Slot	
Size : C	Document Number :		Rev : 3.13
Date: Wednesday, December 09, 2020		Sheet : 47	of 97



Lenovo

Project Name :

Jaguar-1

Title :

dGPU

Size :

C

Document Number :

Rev :

3.13

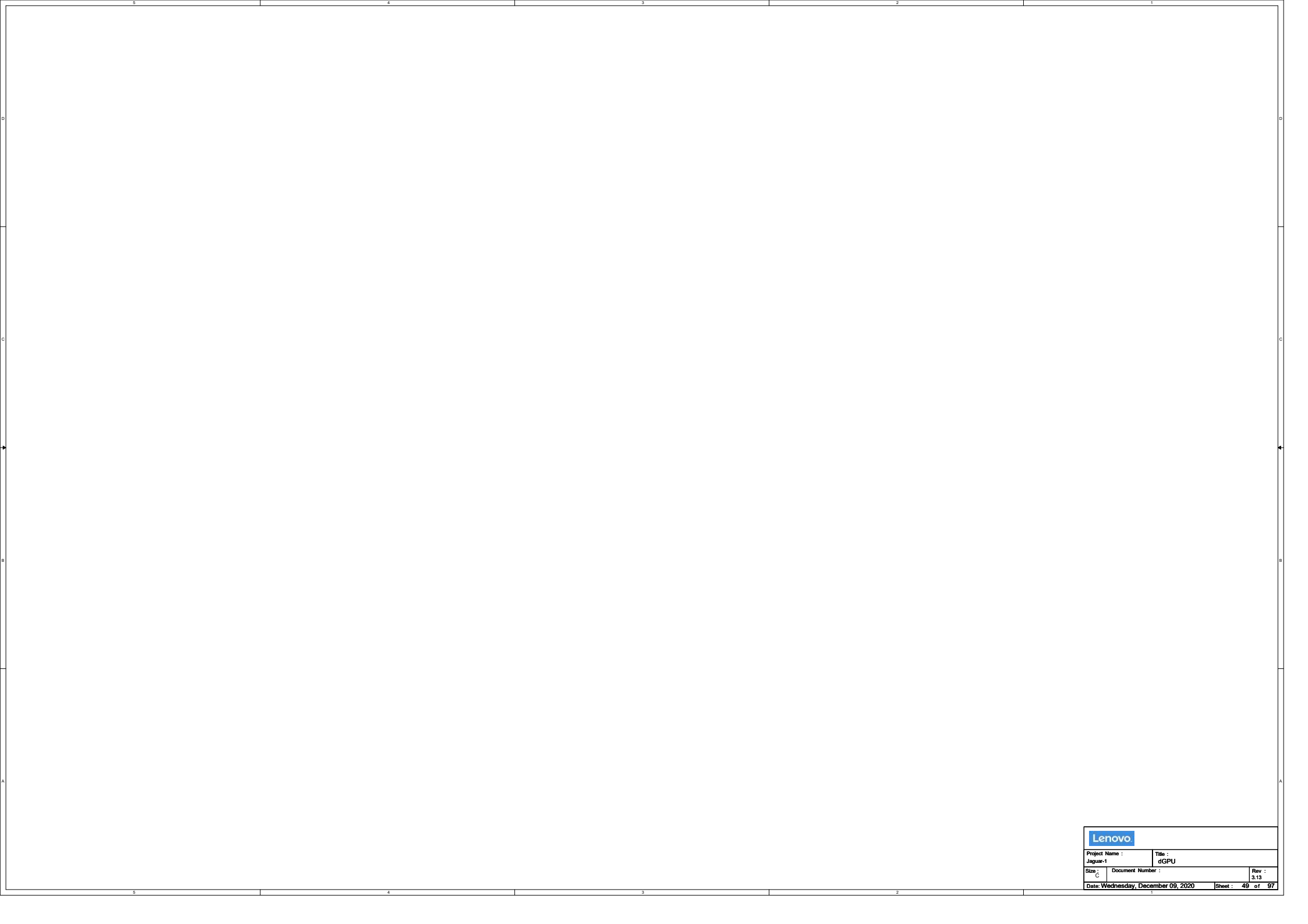
Date: Wednesday, December 09, 2020

Sheet :

48

of


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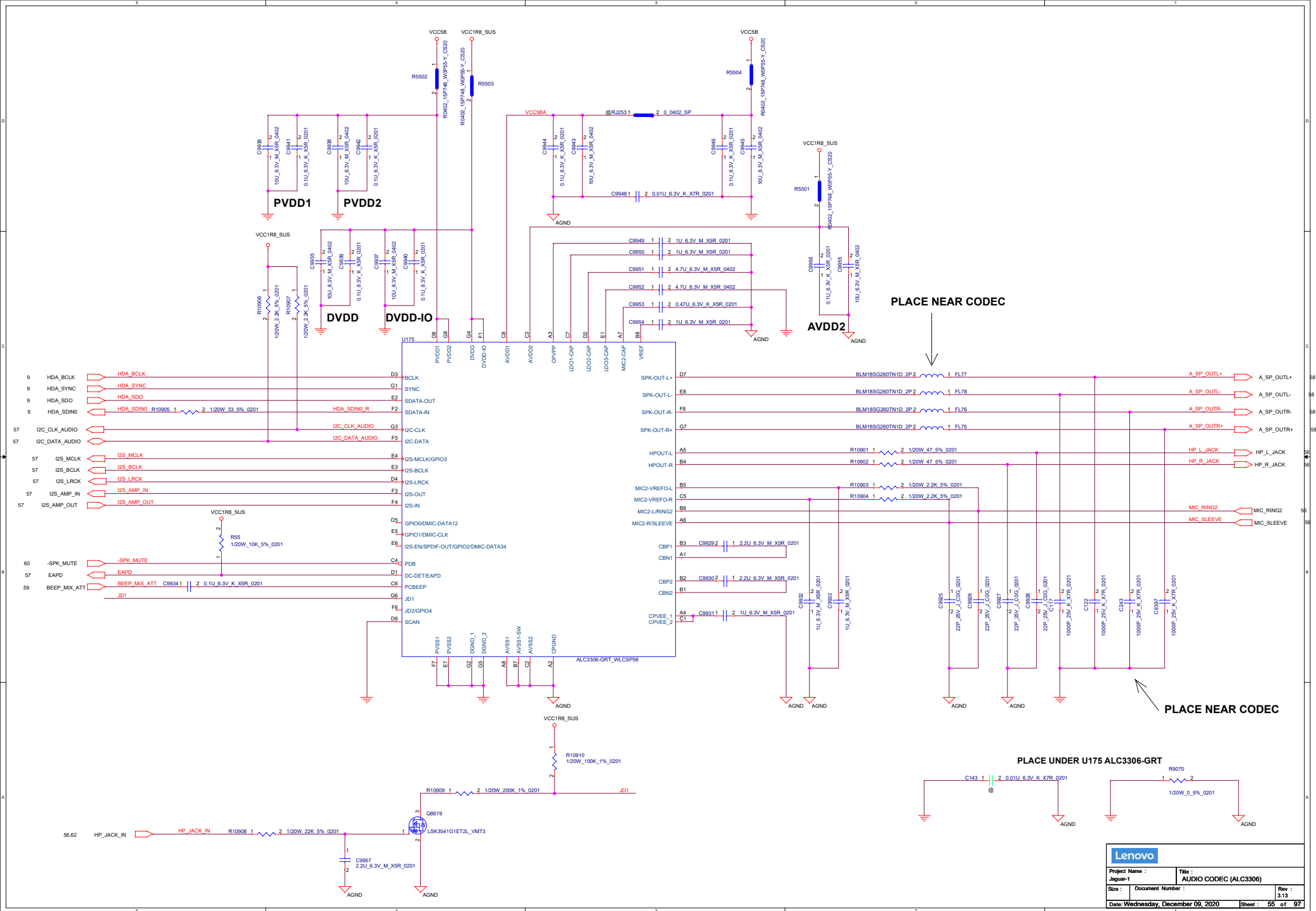


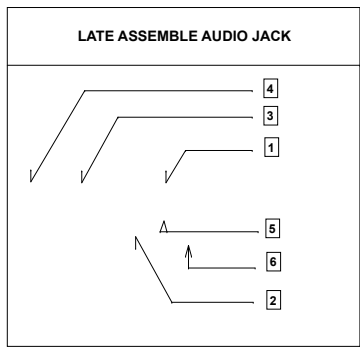
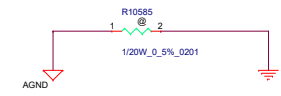
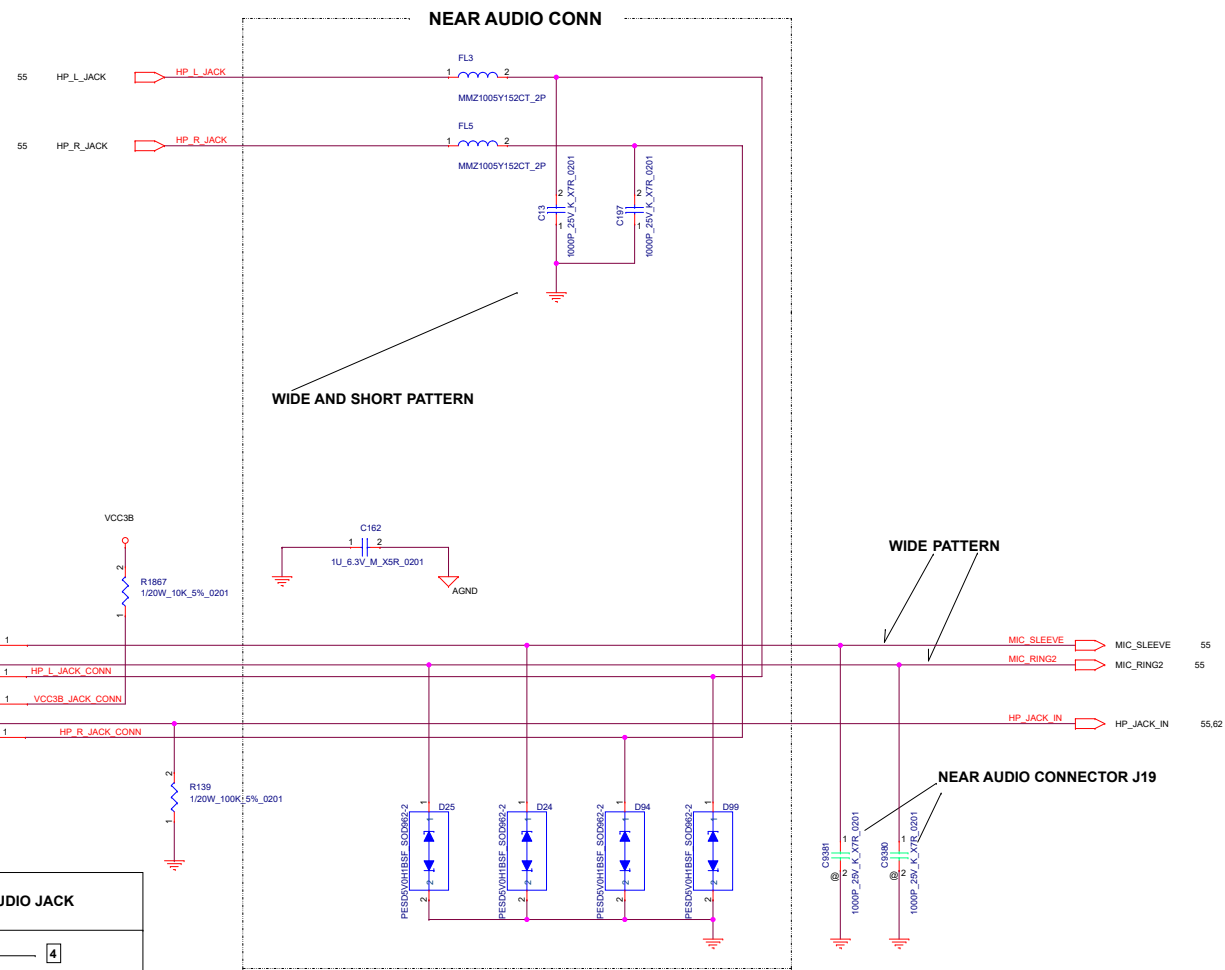
Lenovo

Project Name : Jaguar-1		Title : dGPU	
Size : C	Document Number :		Rev : 3.13
Date: Wednesday, December 09, 2020		Sheet : 49	of 97

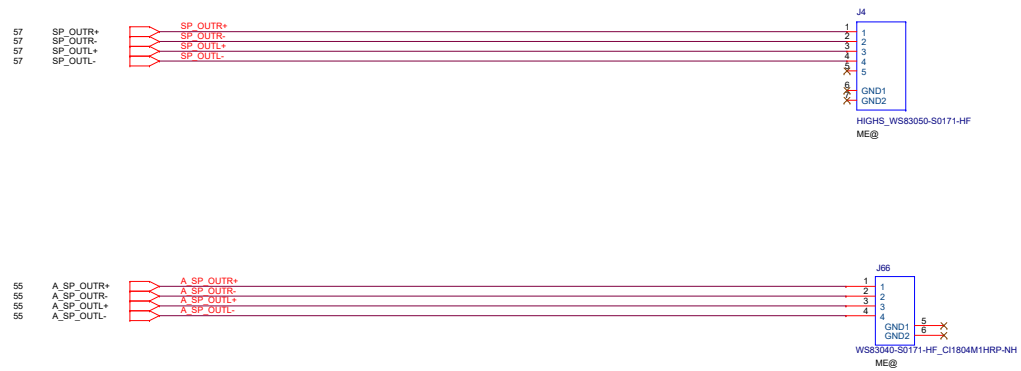
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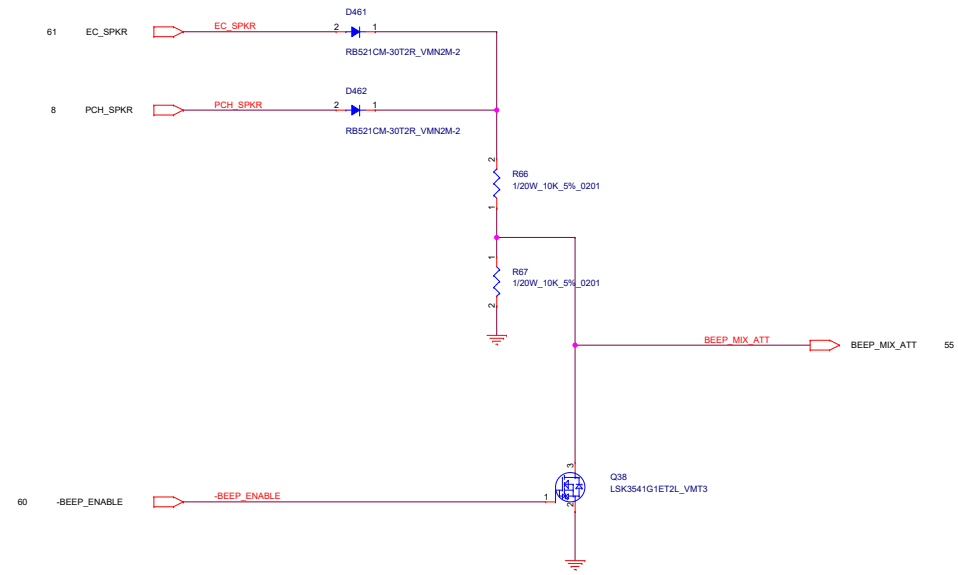
		
Project Name : Jaguar-1		Title : VRAM
Size : C	Document Number :	Rev : 3.13
Date: Wednesday, December 09, 2020		Sheet : 54 of 97





Pin 5 and 6 : Normal Open





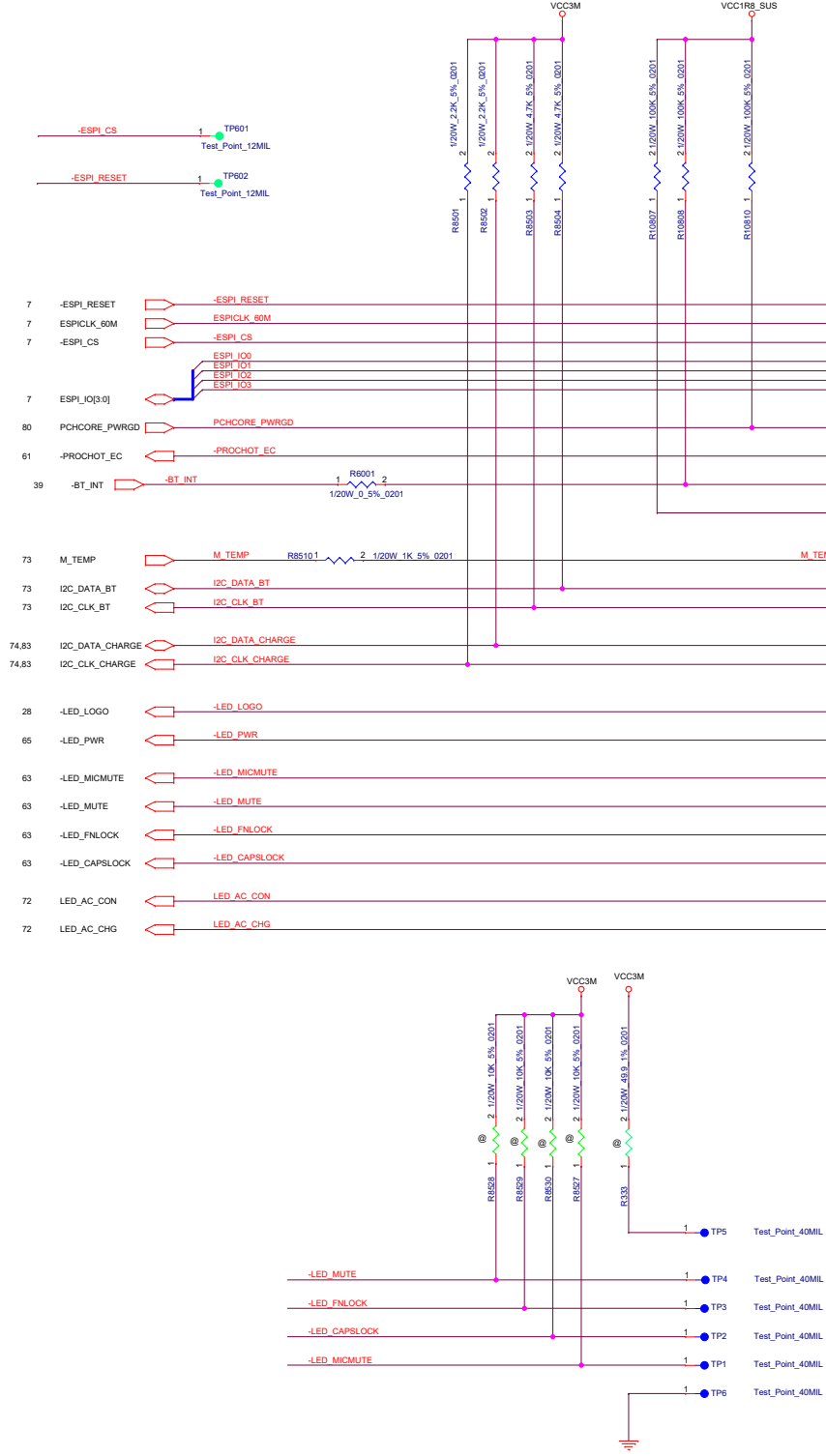


TABLE: EC JTAG Debug Port

Logic	Ref Des	Enable	Disable
Page 60	R333	ASM	NO_ASM
	R8527	ASM	NO_ASM
	R8530	ASM	NO_ASM
	R8529	ASM	NO_ASM
	R8528	ASM	NO_ASM
Page 62	R8714	ASM	NO_ASM
	R8715	No_ASM	ASM

TABLE: Functional Strap

KSO01(Crisis Recovery over keyscan conn)	
HIGH	Normal Boot
LOW	Crash Recovery

← LOGIC

HOST I/F

Battery

LED

TrackPoint

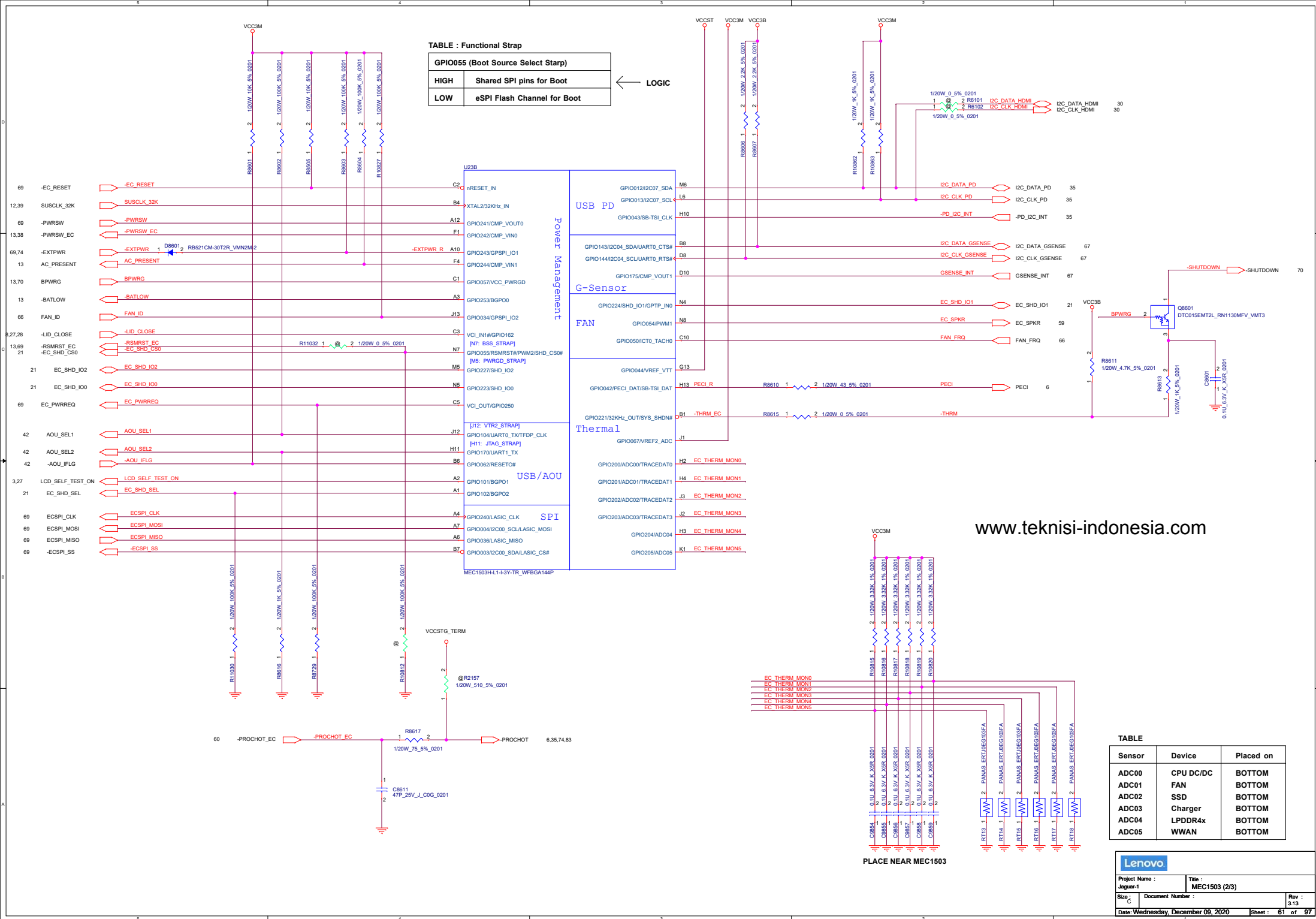
ICD

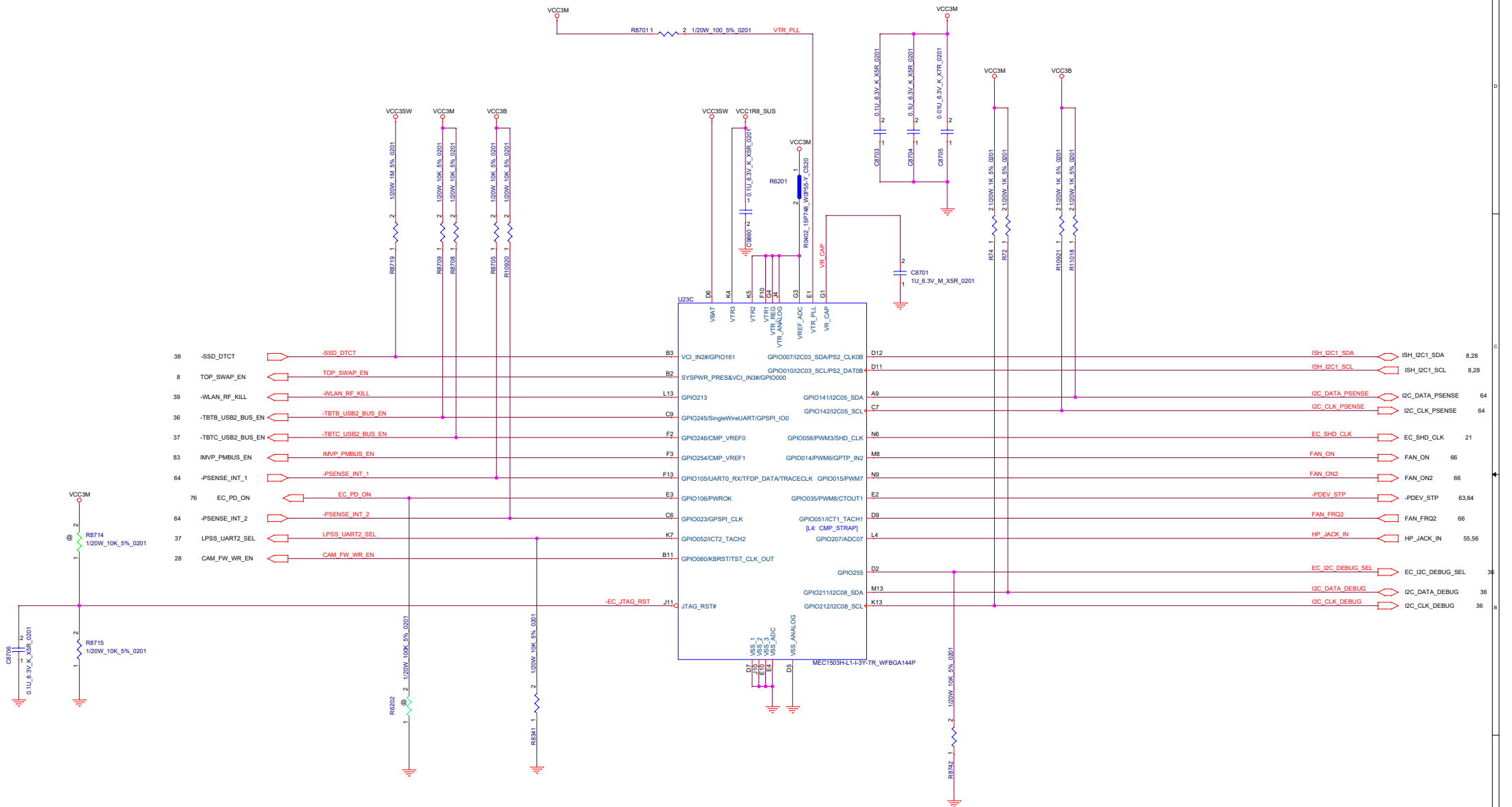
Audio

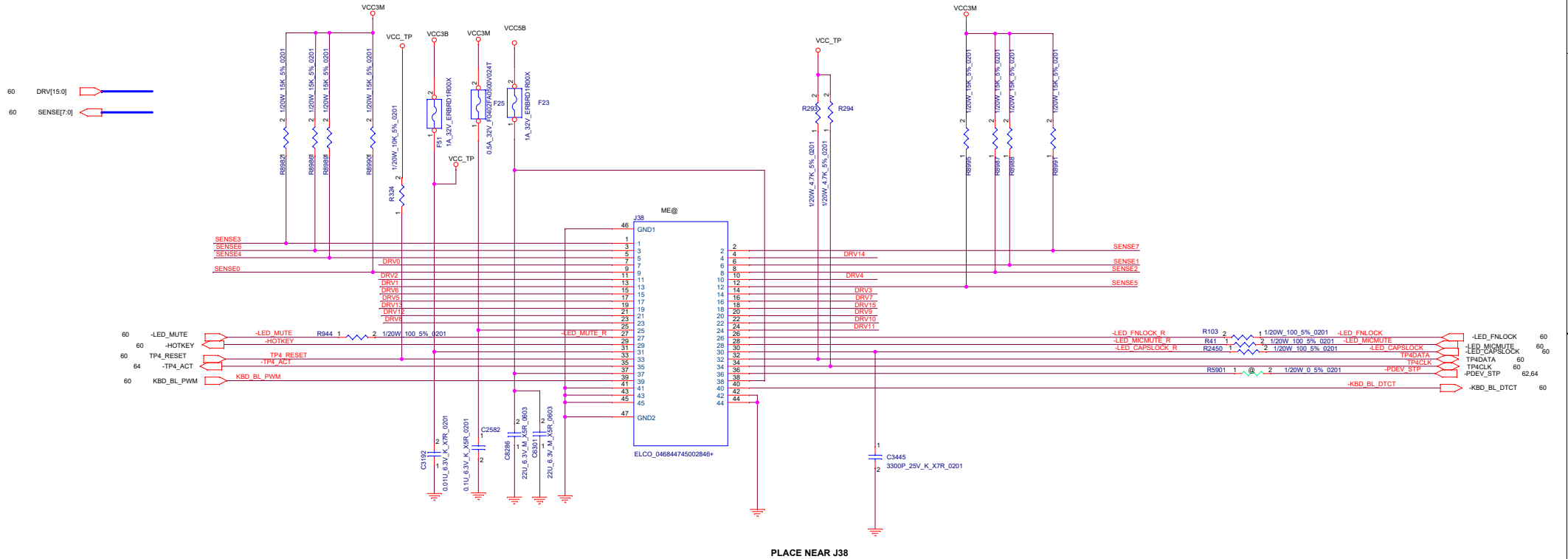
Keyboard

↑ LOGIC

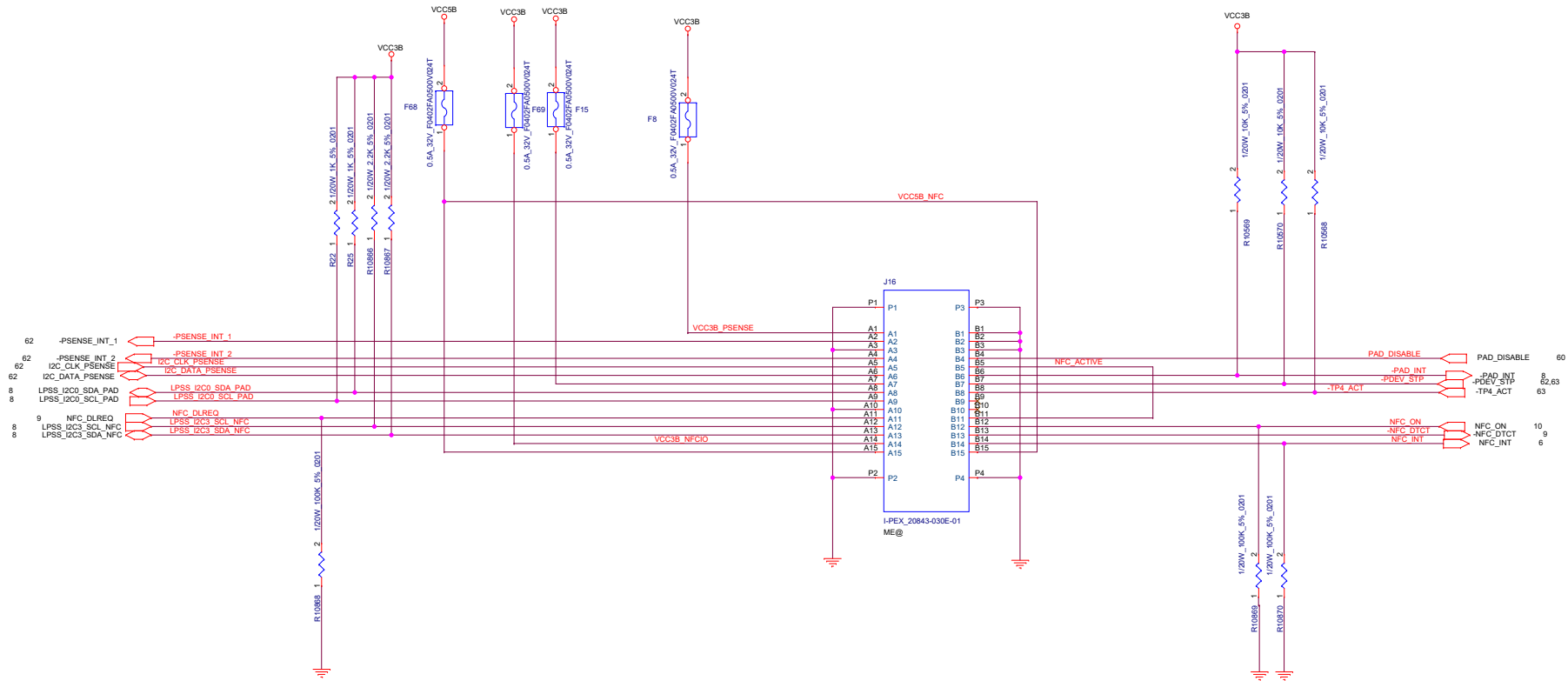
Lenovo

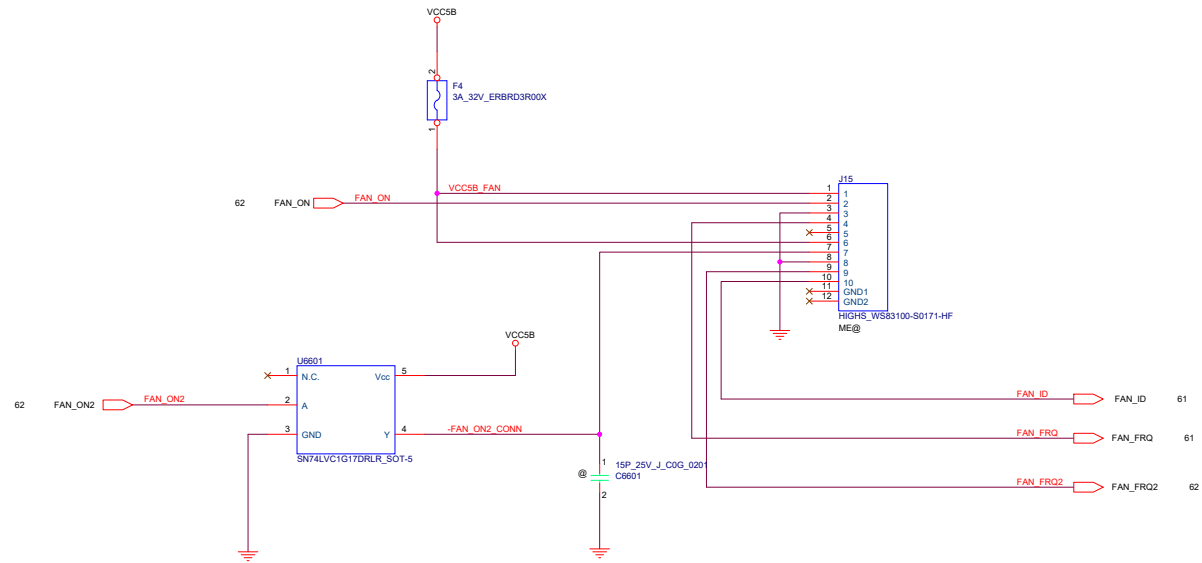






PLACE NEAR J38

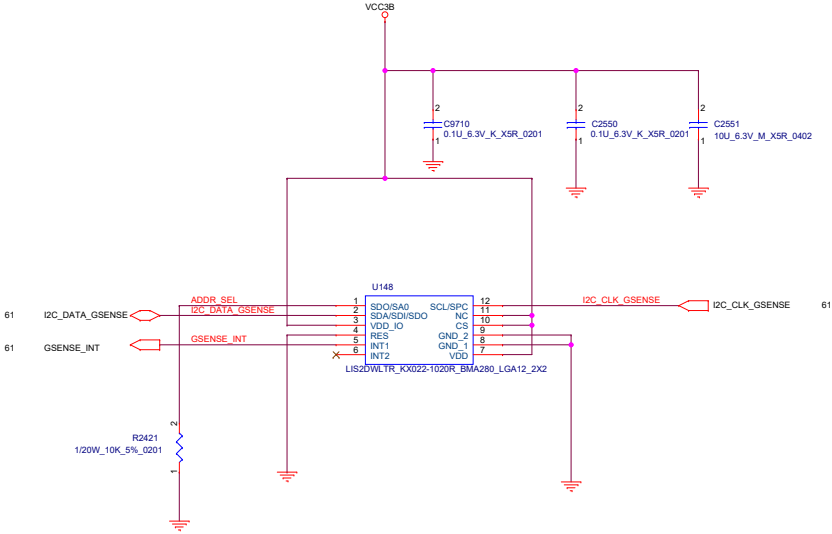




TABLE

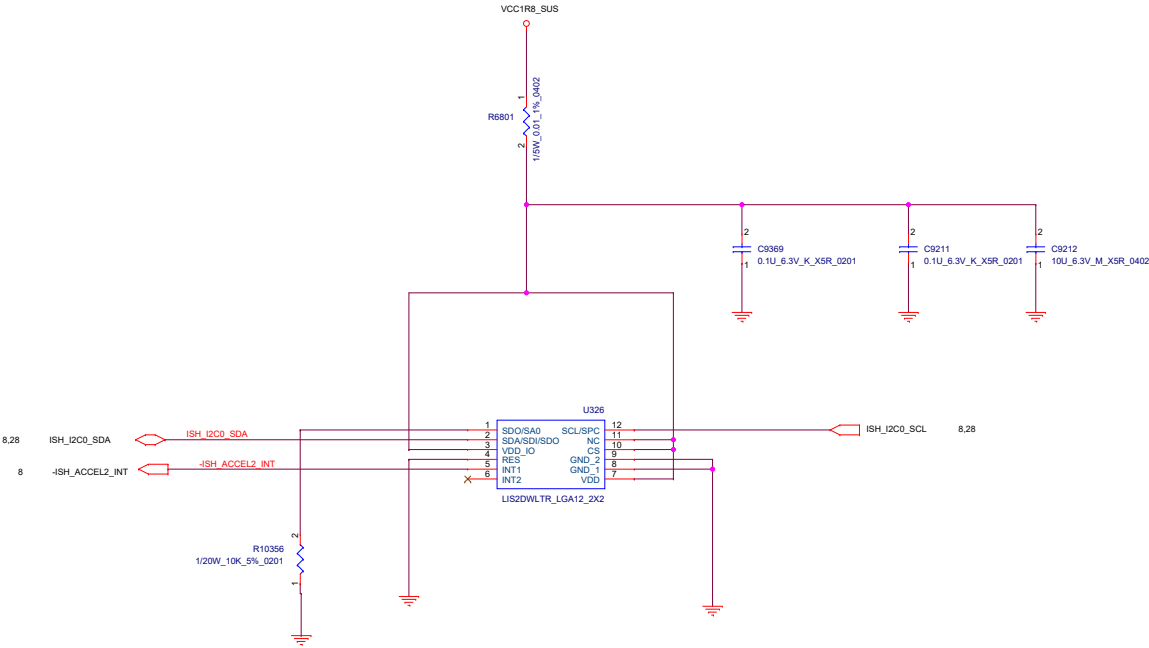
P/N	ADDR_SEL	Address
LIS2DWL	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
BMA280	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)

ST and Bosch I2C address is same but can be identified by Chip_ID

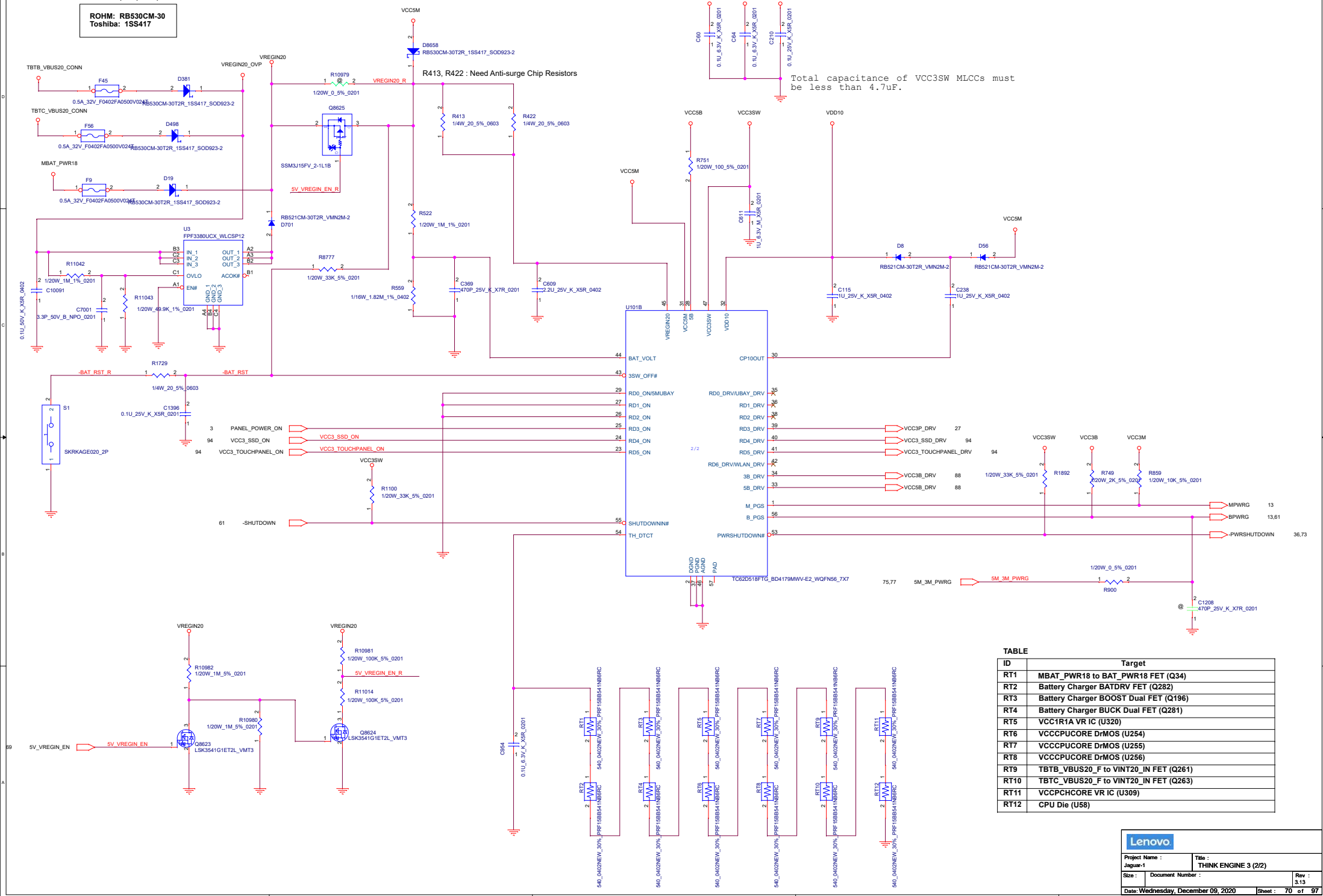


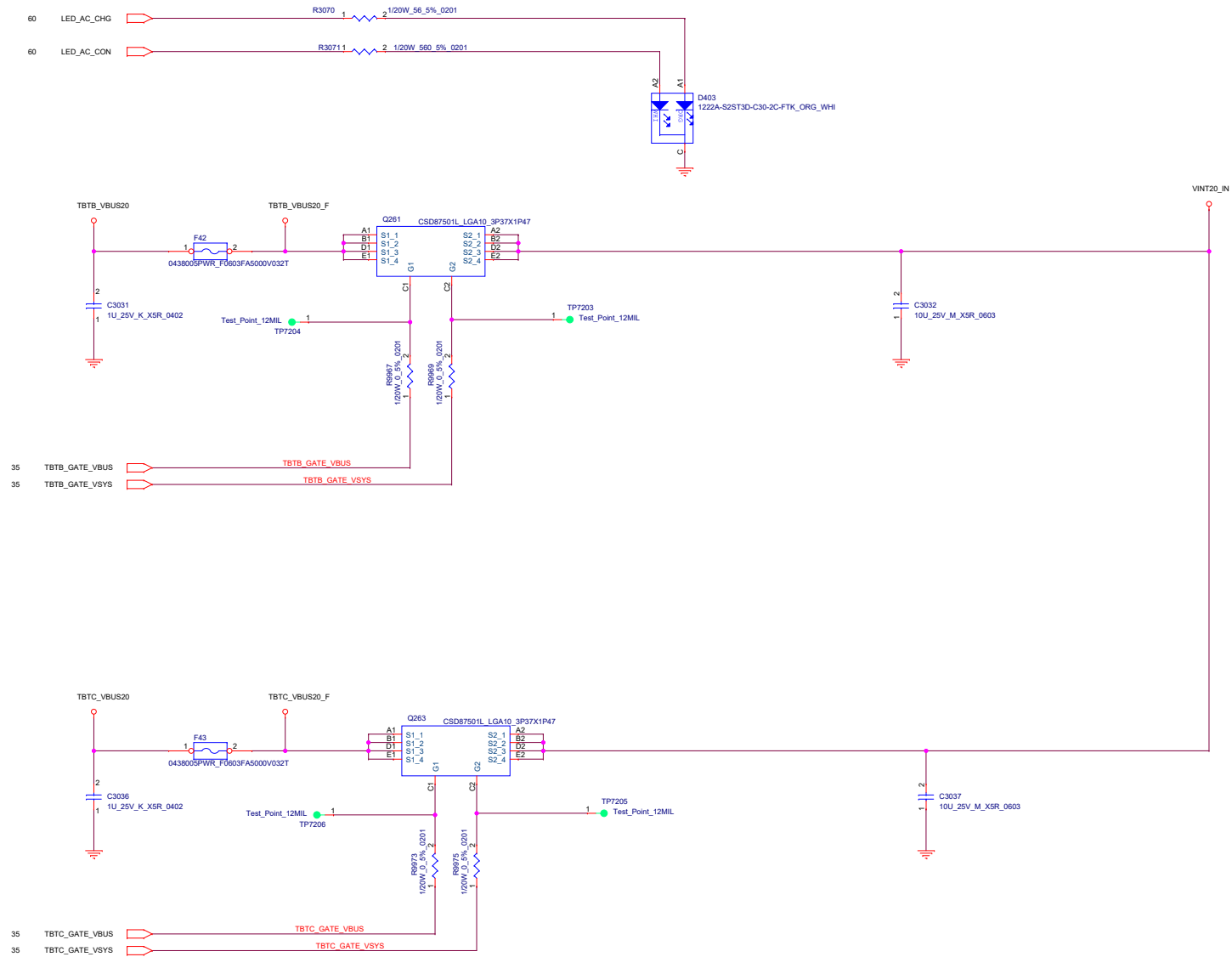
TABLE

P/N	ADDR_SEL	Address
LIS2DWL	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)



ROHM: RB530CM-30
Toshiba: 1SS417





Lenovo

Project Name : Jaguar-1		Title : DC INPUT	
Size : C	Document Number :		Rev : 3.13
Date: Wednesday, December 09, 2020		Sheet : 72 of 97	

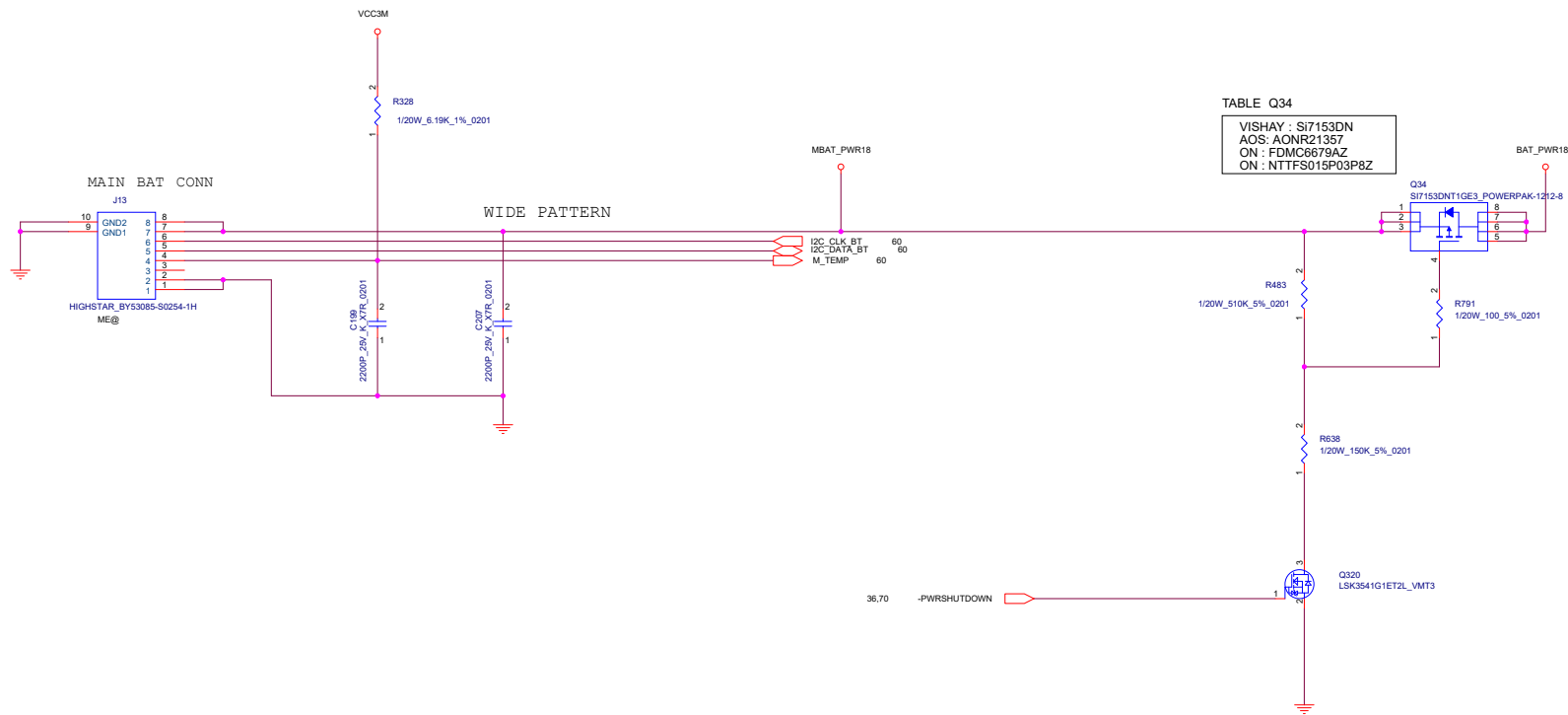
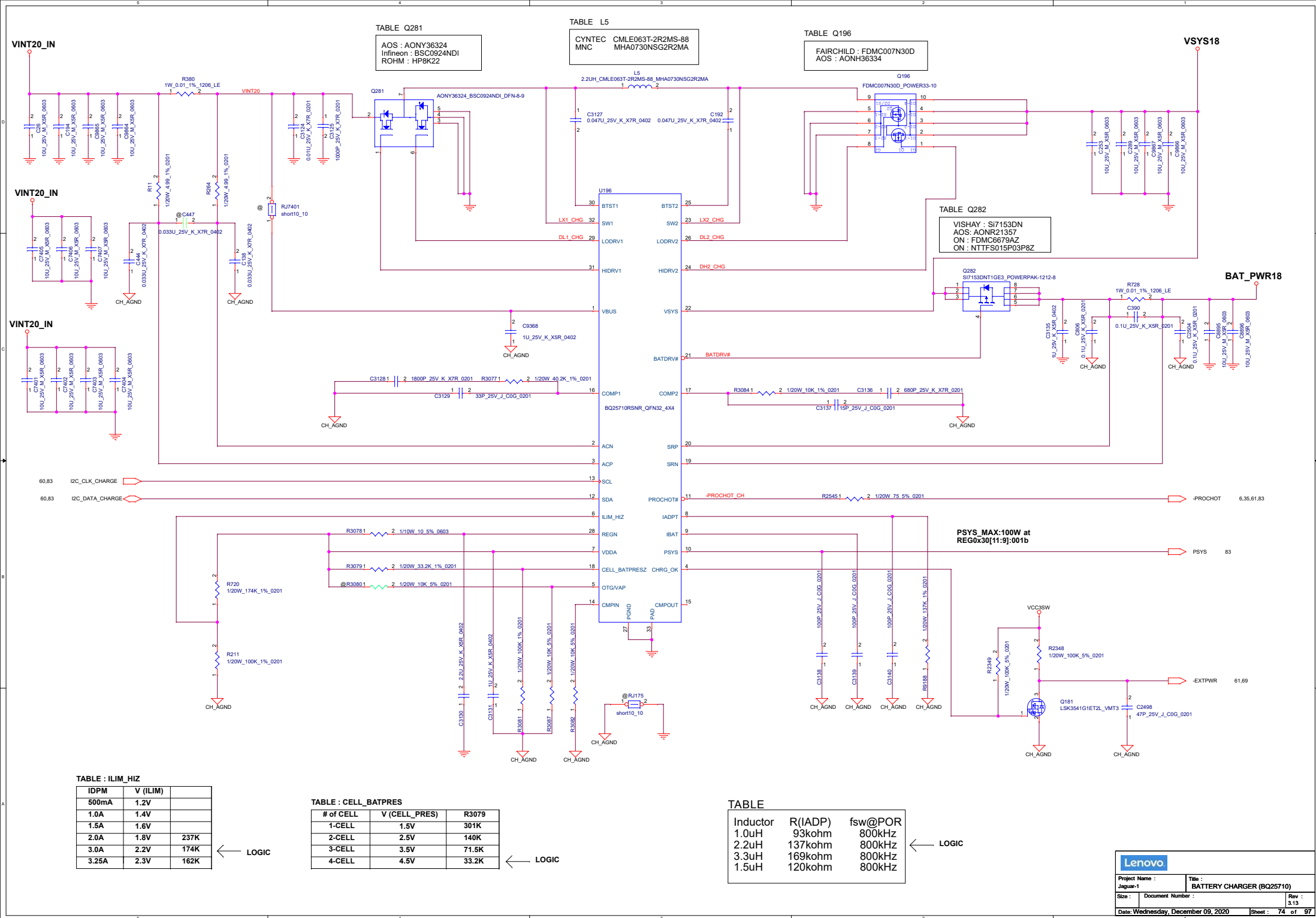


TABLE Q34

VISHAY : Si7153DN
AOS : AONR21357
ON : FDMC6679AZ
ON : NTTFS015P03P8Z

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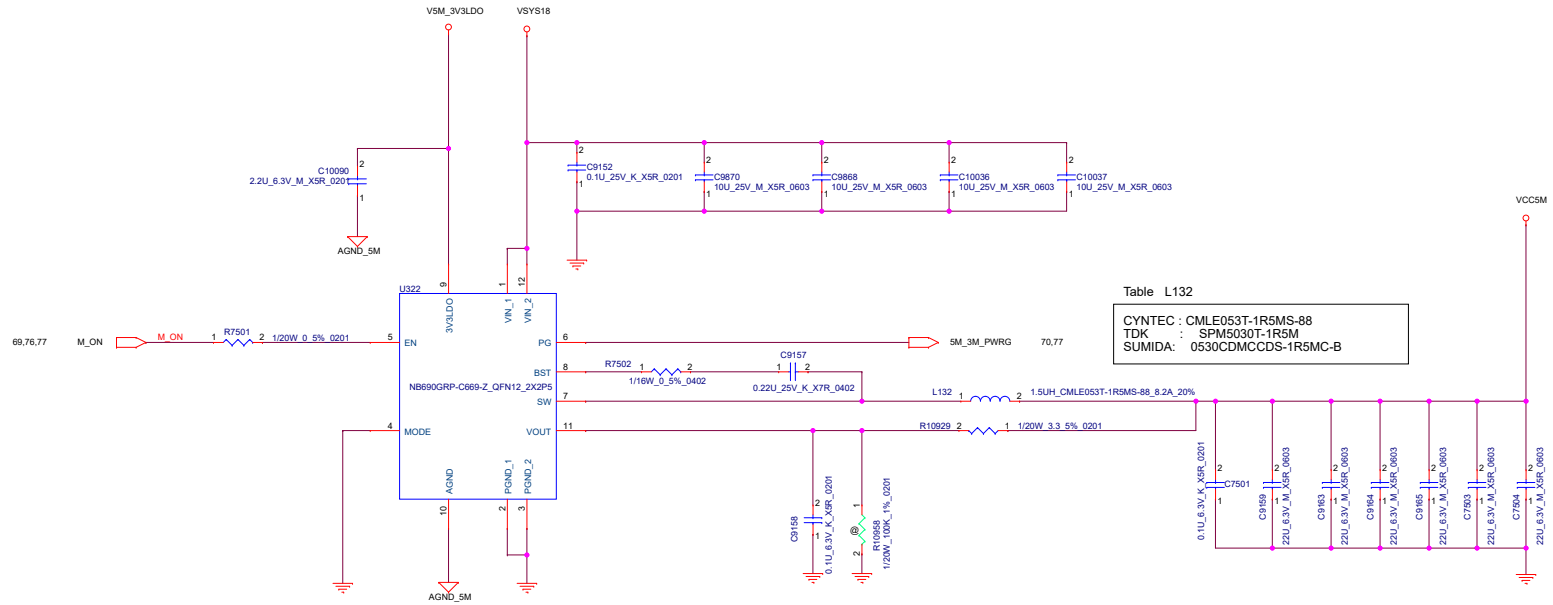


TABLE: NB690 Mode Control

RMode	MODE	VOUT	3V3LDO
0	Ceramic Cout	5.1V	3.3V
60K	POSCAP Cout	5.1V	3.3V
120K	Ceramic Cout	5V	3.3V
180K	POSCAP Cout	5V	3.3V
Floating	X	3.3V	3.3V

← LOGIC

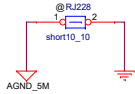


Table L132

CYNTEC :	CMLE053T-1R5MS-88
TDK :	SPM5030T-1R5M
SUMIDA :	0530CDMCCDS-1R5MC-B

TABLE : NB693 Mode Control

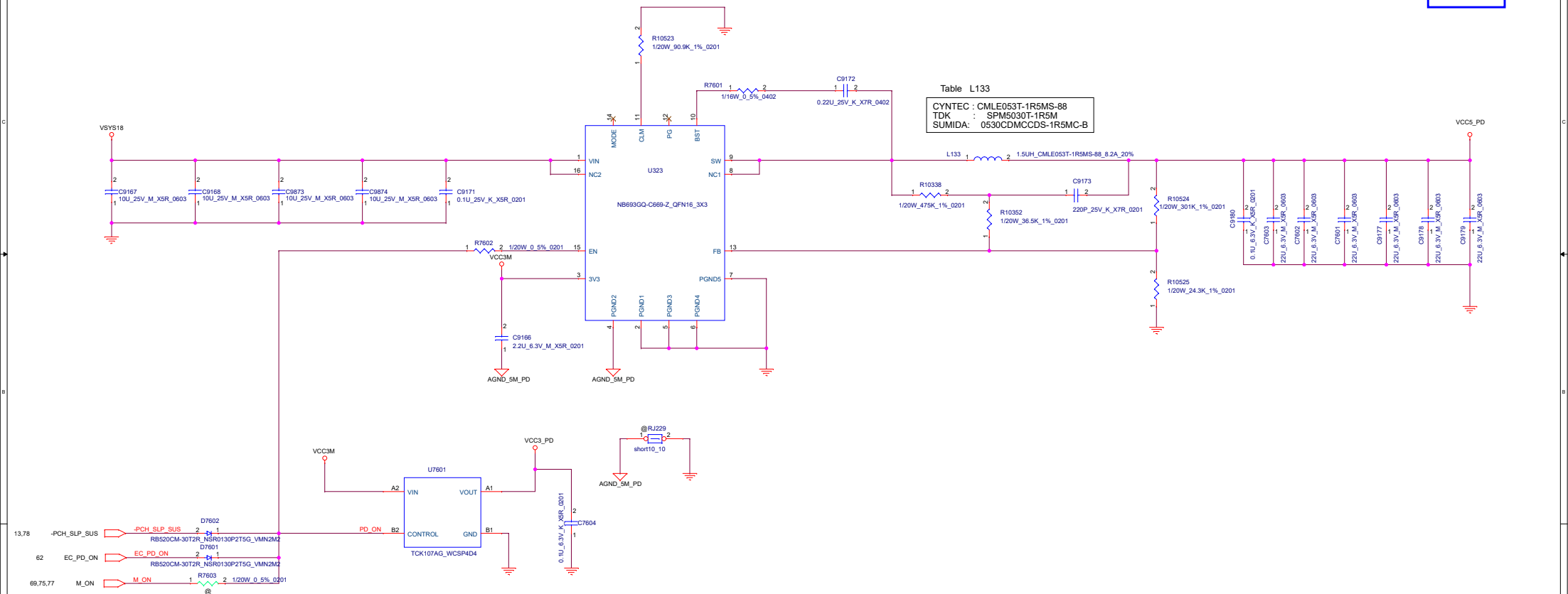
Mode	VOUT		RMode
M1	Vo<3V	DCM	0
M2	Vo<3V	CCM	90K
M3	Vo>=3V	CCM	150K
M4	Vo>=3V	DCM	>230K or Float

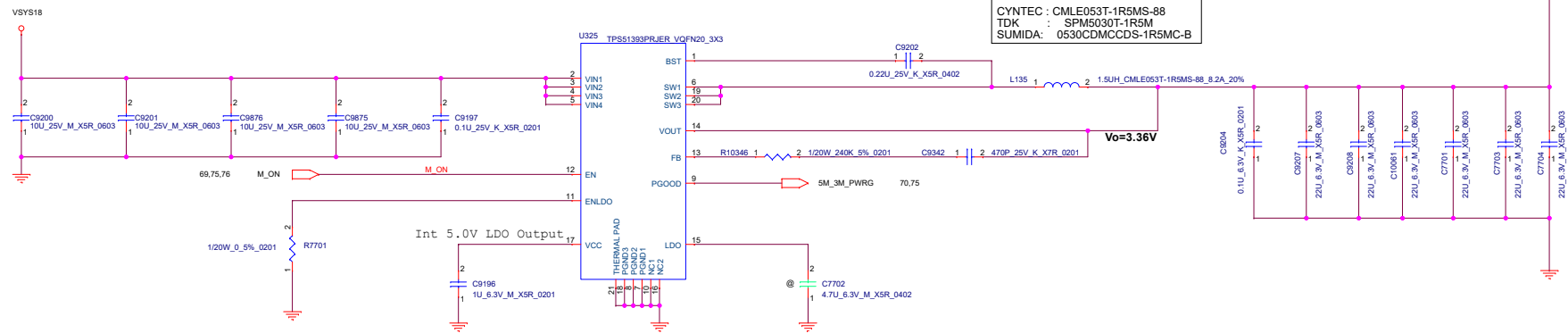
← LOGIC

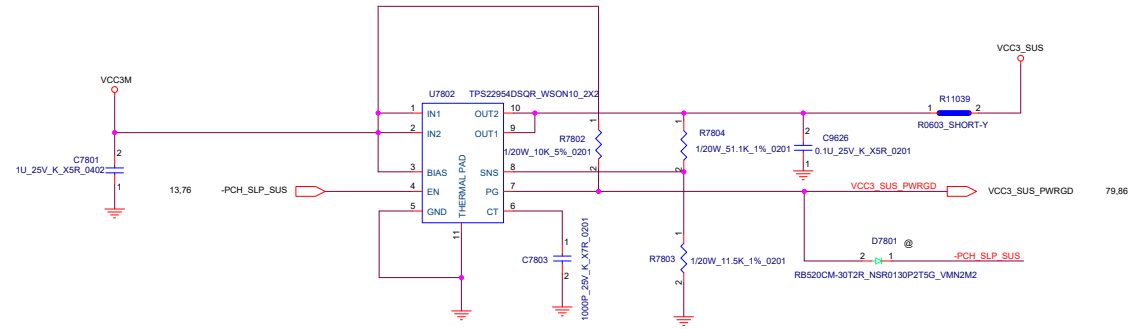
VCC5M_PD
5.3V / 6.3A

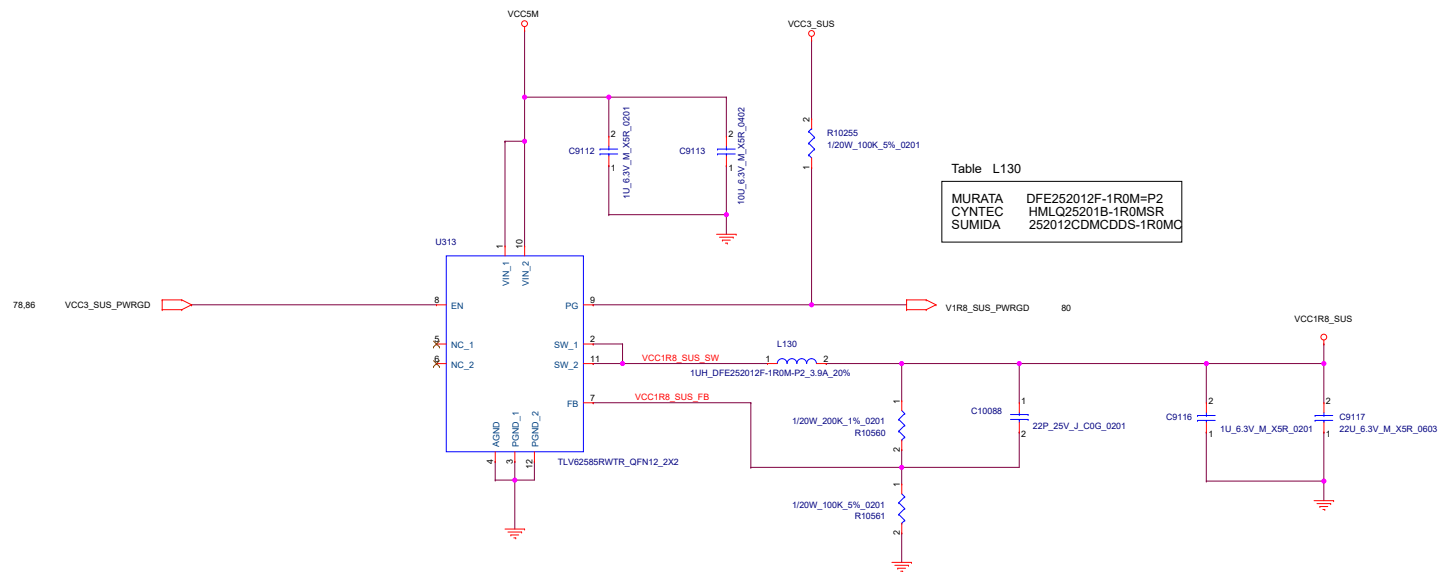
Table L133

CYNTEC : CMLE053T-1R5MS-88
TDK : SPM5030T-1R5M
SUMIDA : 0530CDMCCDS-1R5MC-B

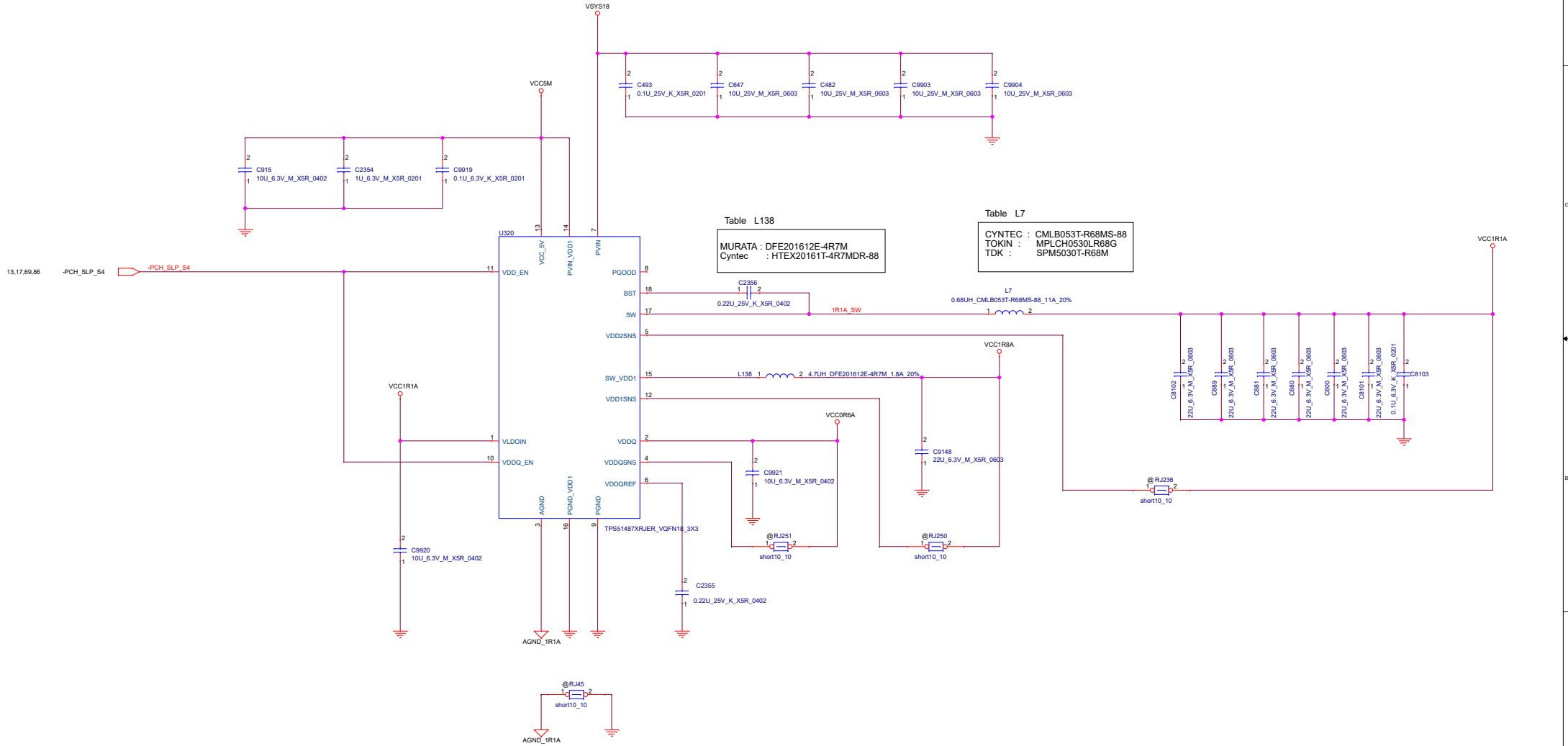








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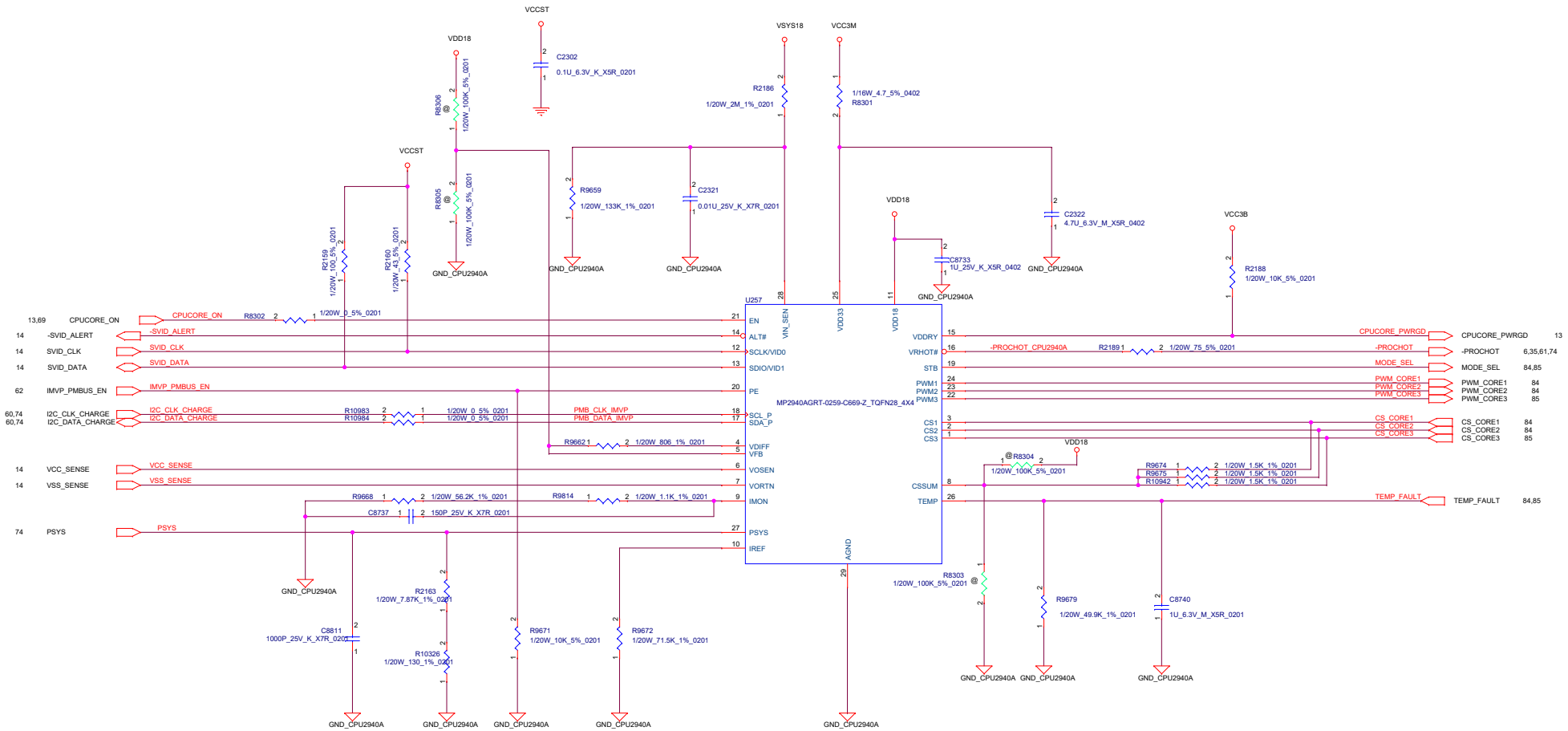
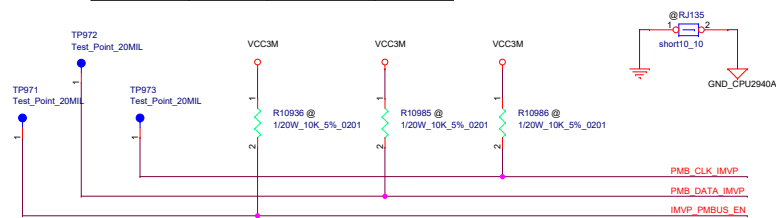
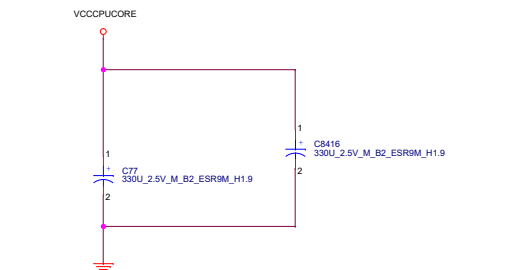
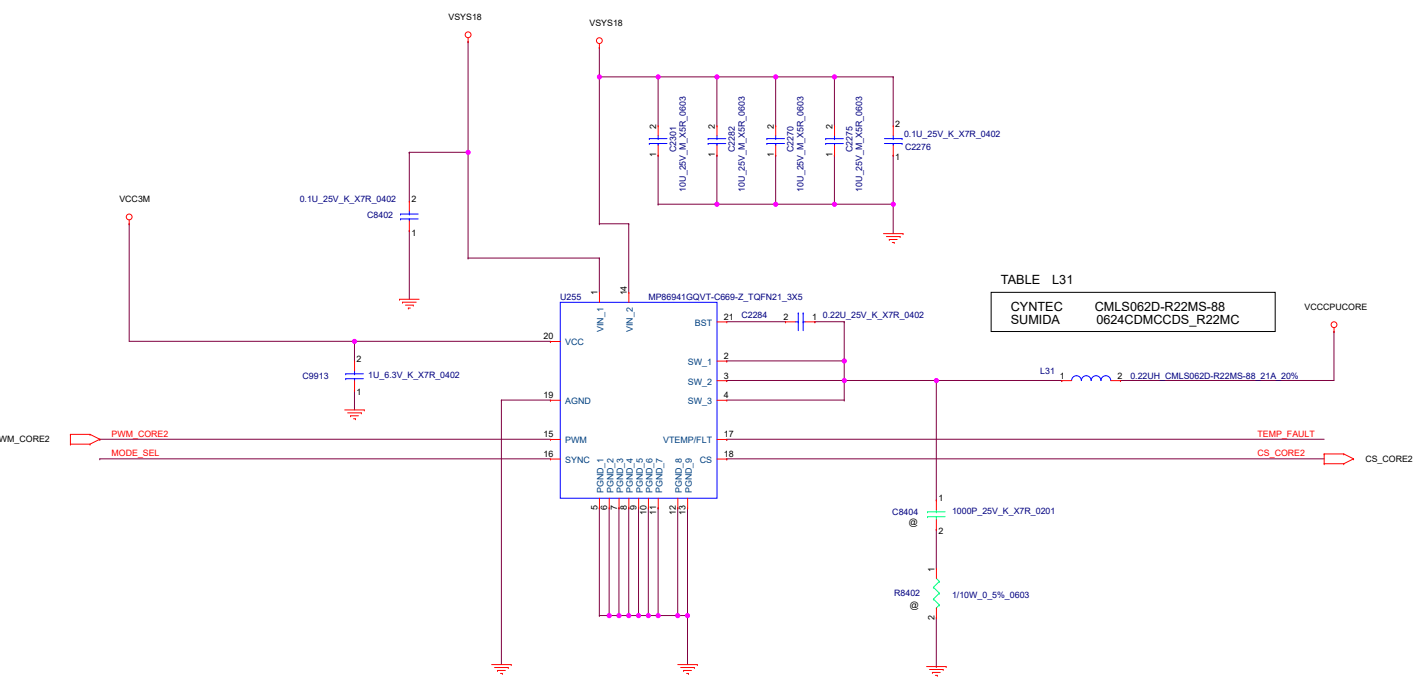
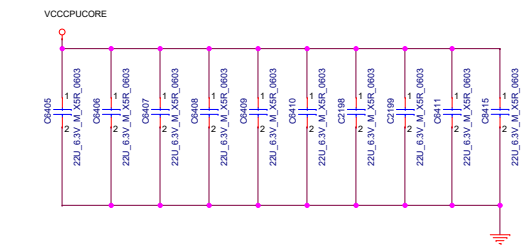
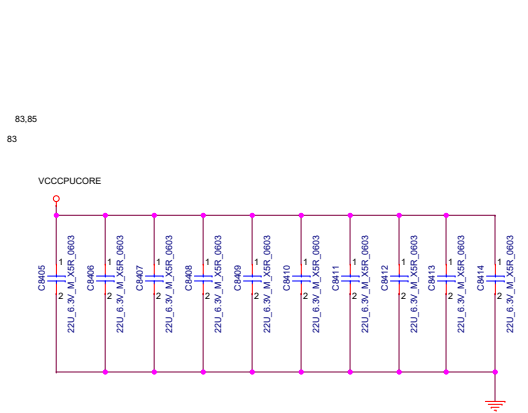
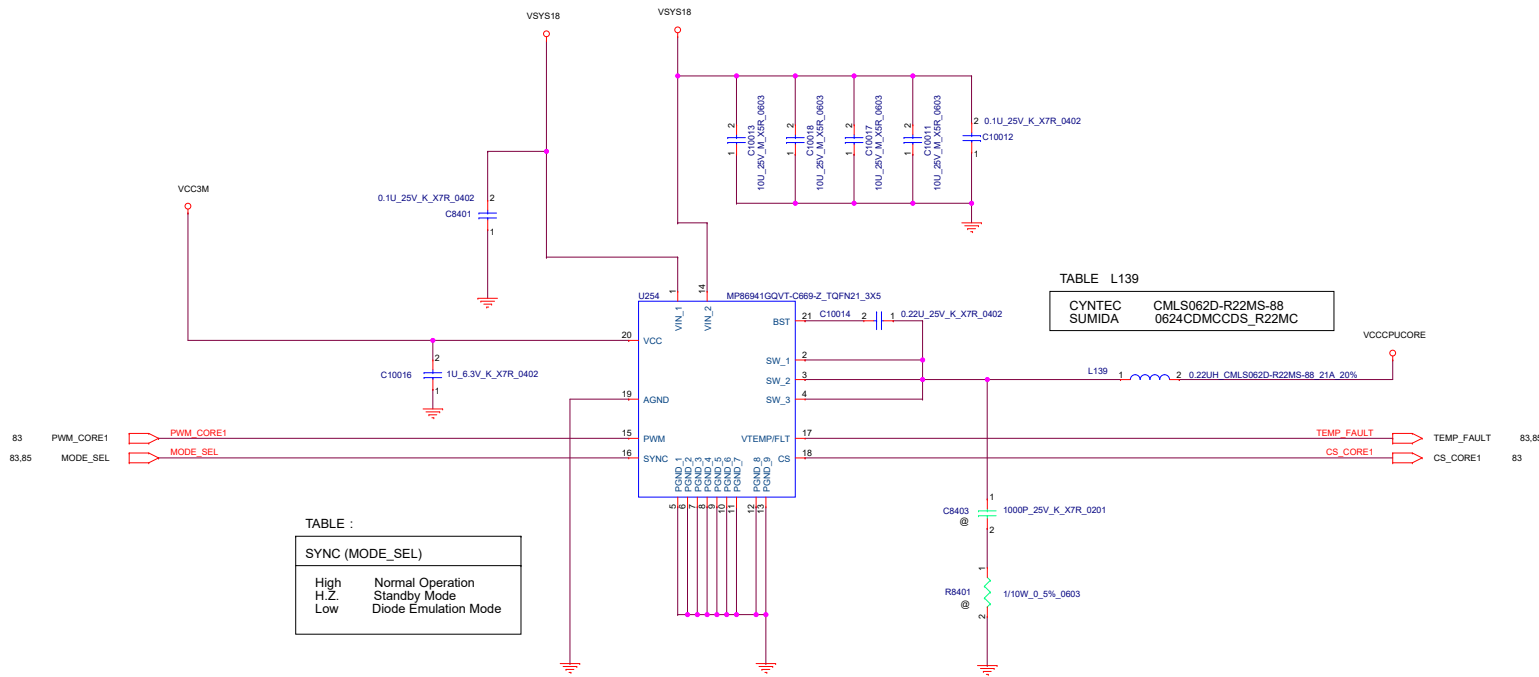


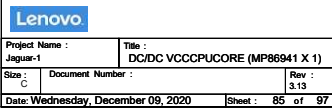
TABLE : PSYS Pull Down Resistor (RPSYS)

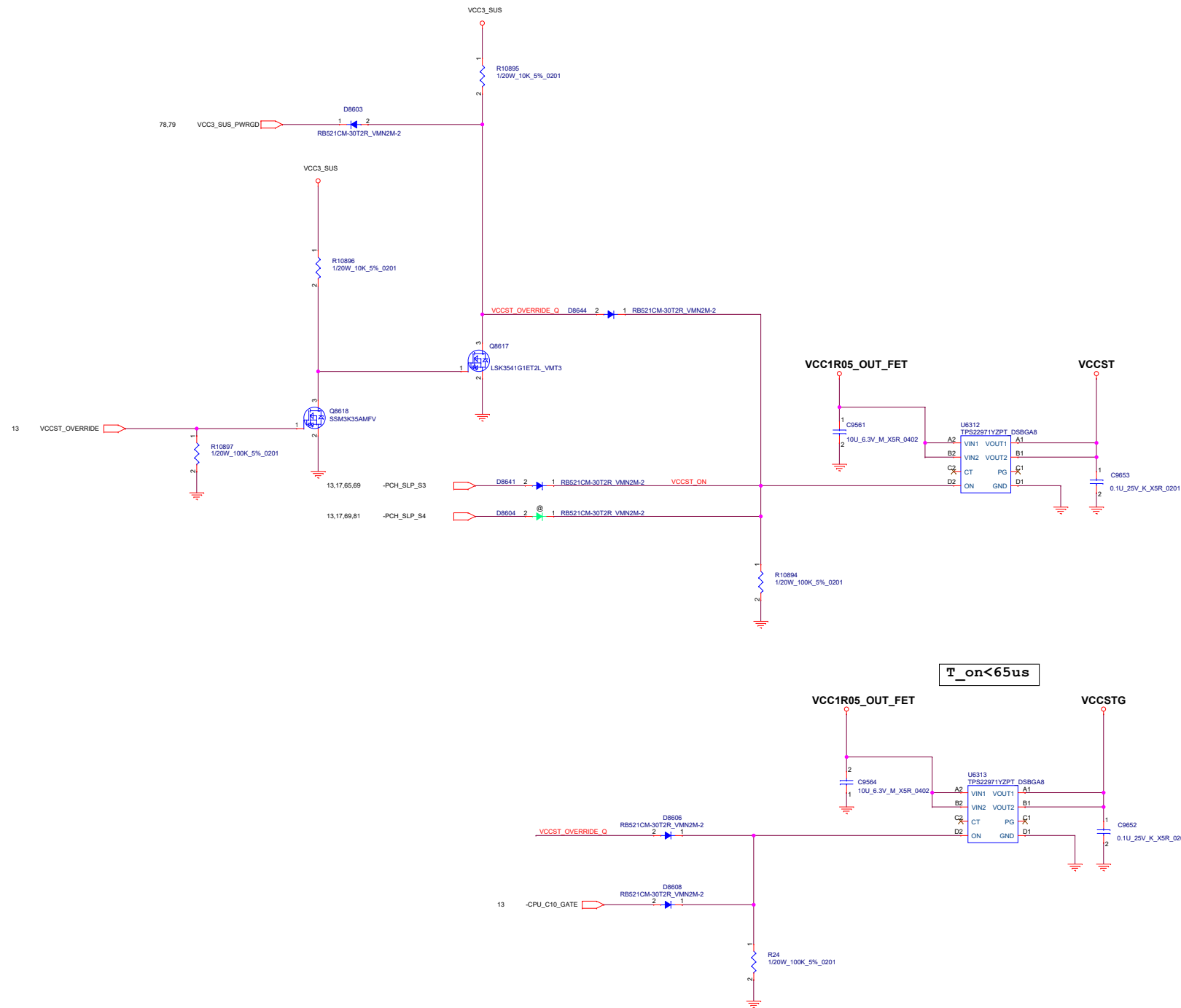
RPSYS = ADC VREF / (IPSYS * PSYS_PMAX)			
ADC VREF	IPSYS	PSYS_PMAX	RPSYS
0.8V	1uA/W	100W	8K-ohm



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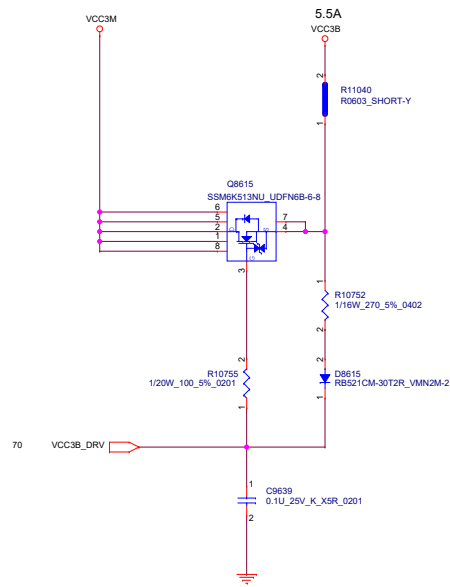




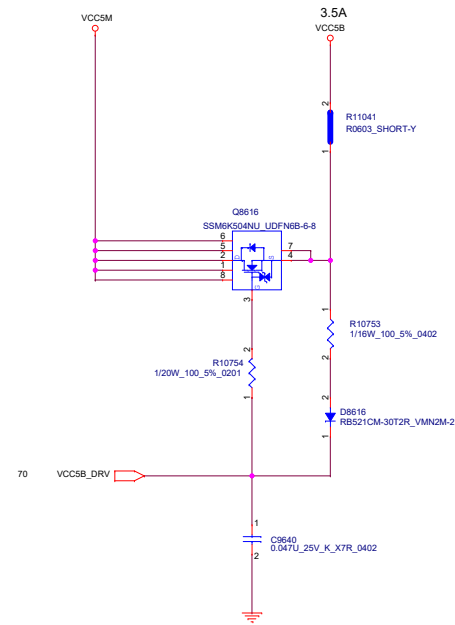


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Q8615
TOSHIBA : SSM6K513NU
FAIRCHILD : FDMA8878
AOS : AON2420

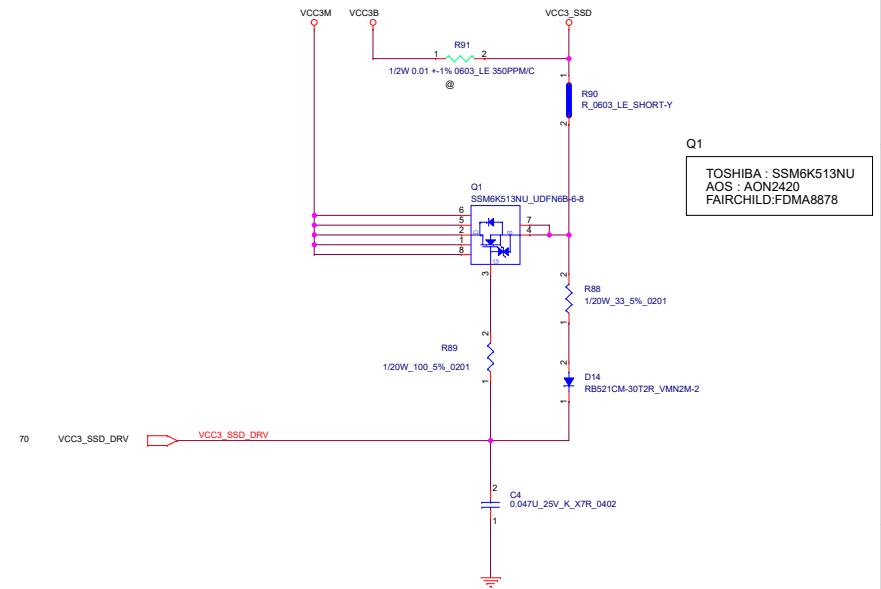
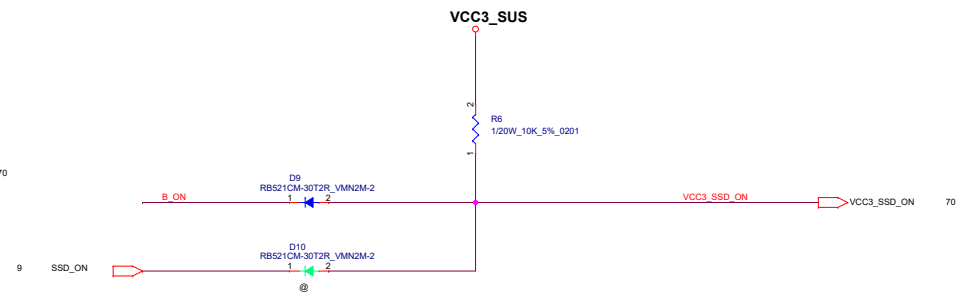


Q8616
TOSHIBA : SSM6K504NU
AOS : AON2420
ROHM : RF4E080BNTR



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FID
Board Area

